

COMPAL CONFIDENTIAL

MODEL NAME : *HBT10*
COMPAL P/N : *DA600001K10*
PCB NO : *LA-2811*
Revision : *1.0*

Sakhir 10E

LA-2811 Rev1.0 Schematic

HBT10 Schematics Document
uFCBGA/uFCPGA Mobile Dothan
ATI RL300MB + SB200(IXP150)
2005-05-04<A>

Function/B
LS-2811

LAN/B
LS-2812

M/B LA-2811

USB/B
LS-2813

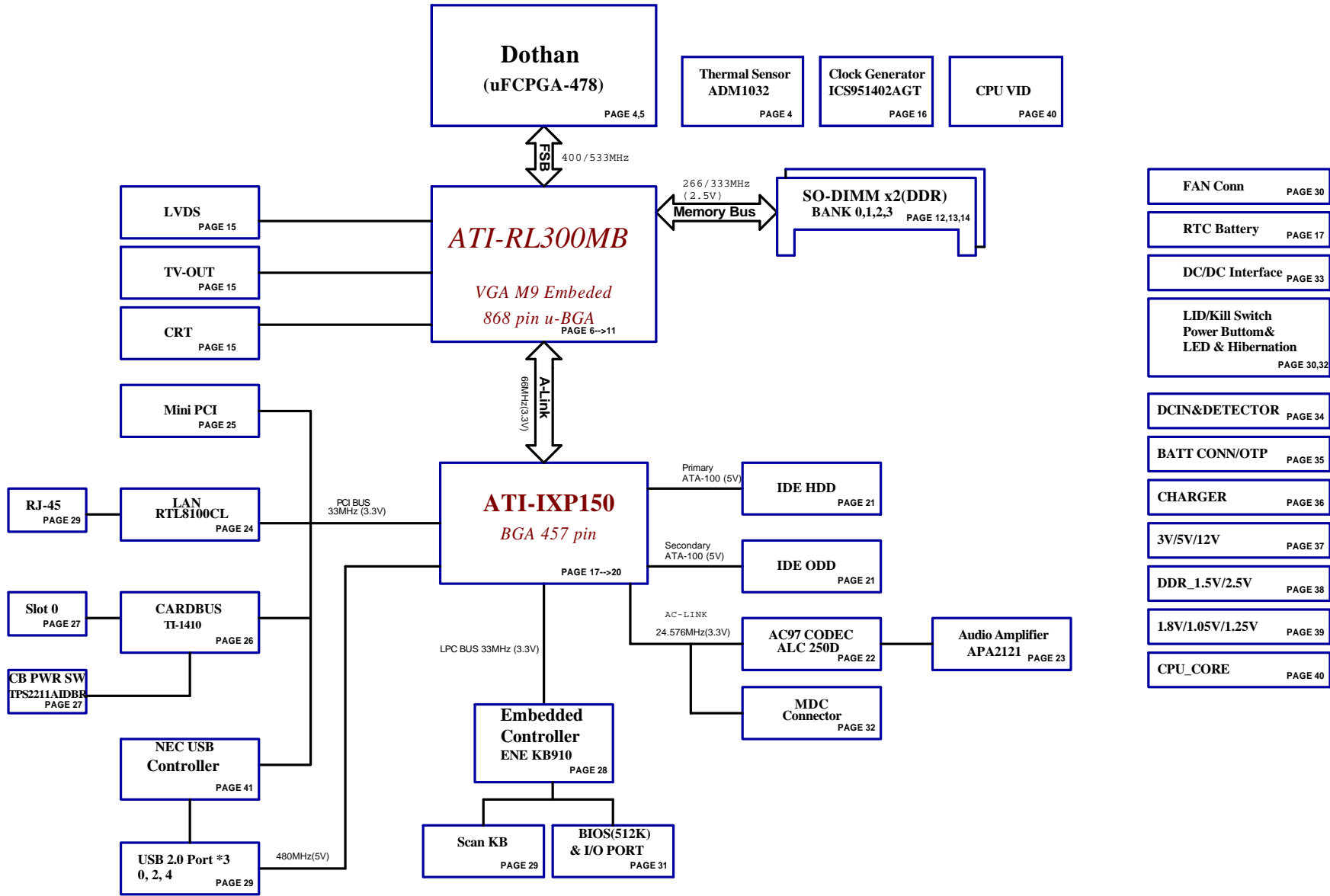
TP/B
LS-2814

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BLOCK DIAGRAM

Model Name : HBT10

File Name : LA-2811 Rev: 0.1



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PC11	AD18	1(for Wireless Lan)	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02) (24C04)	1010 000X b 1011 000Xb		

EC SM Bus2 address

IXP150 SM Bus address

Device	Address
Clock Generator (1CS951402AGT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

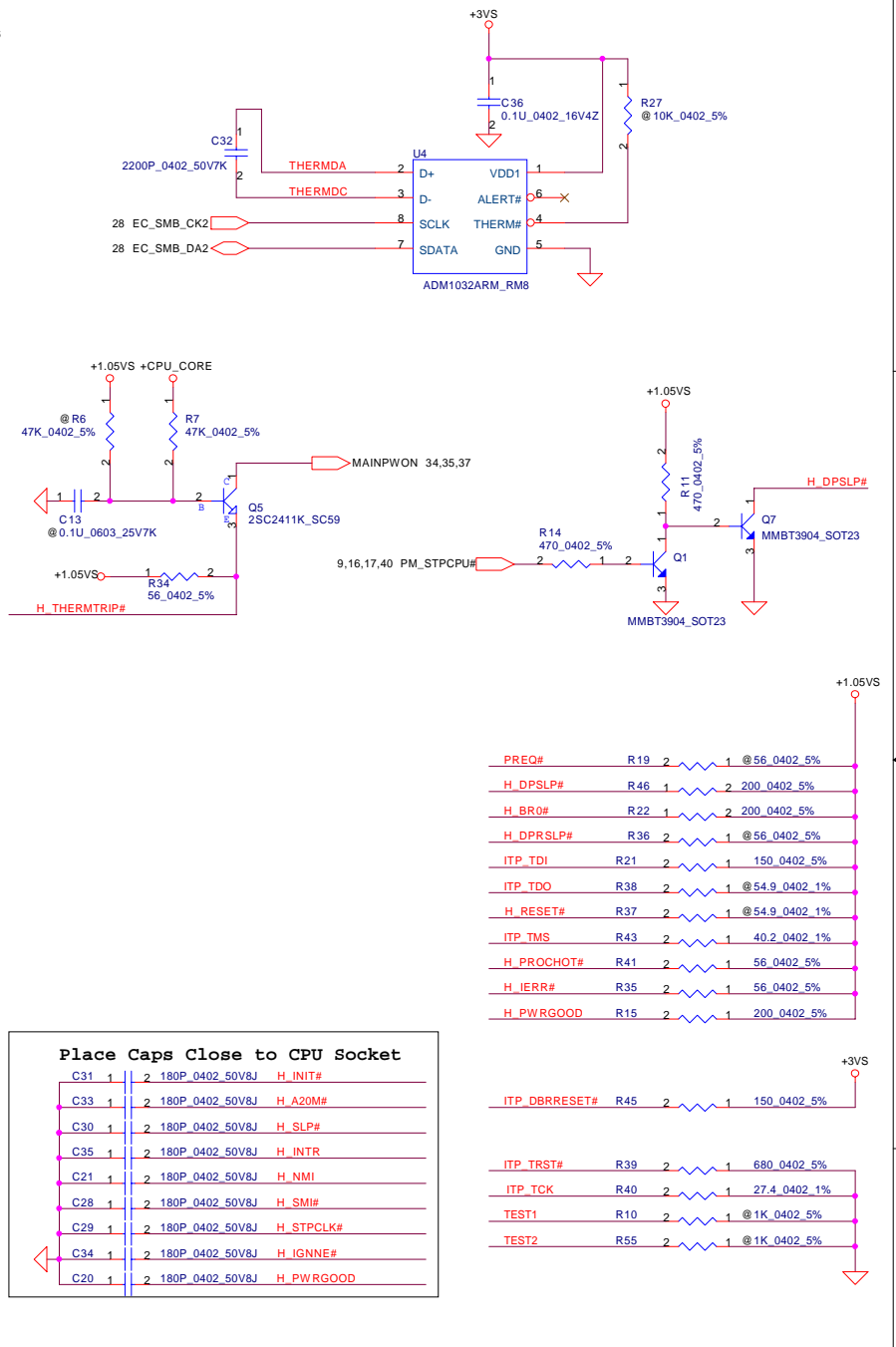
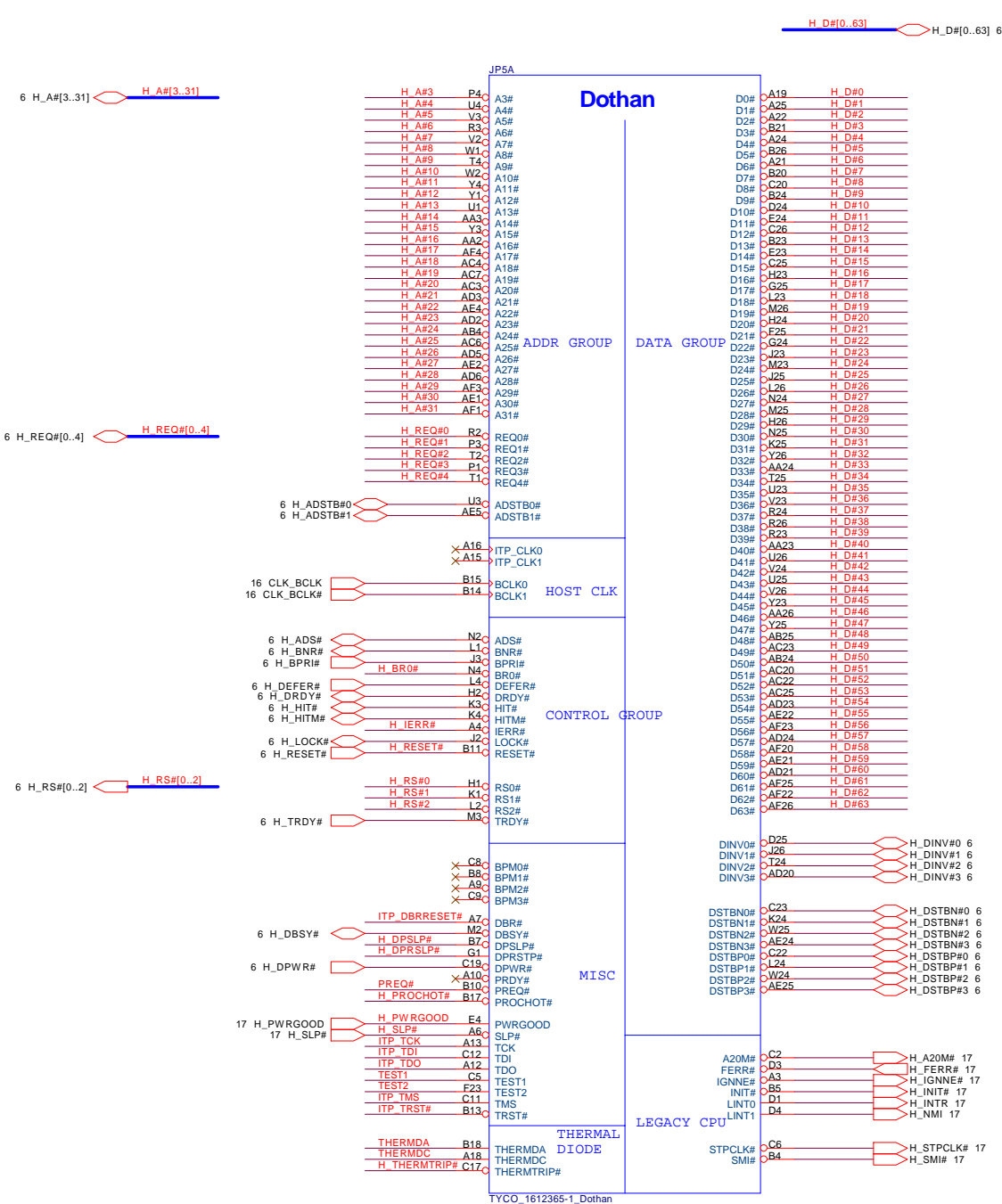
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table

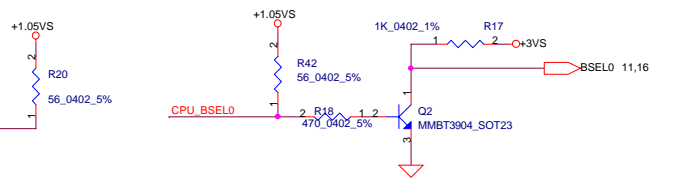
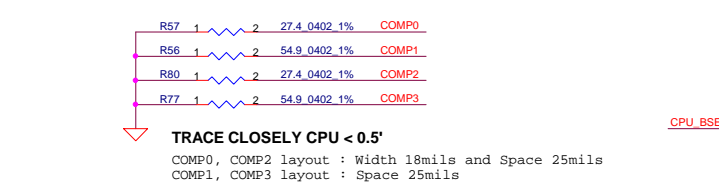
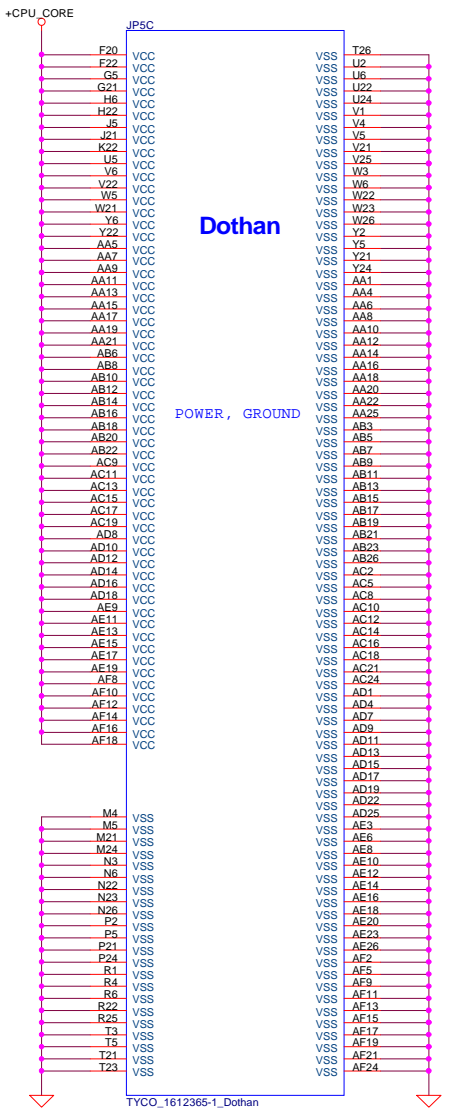
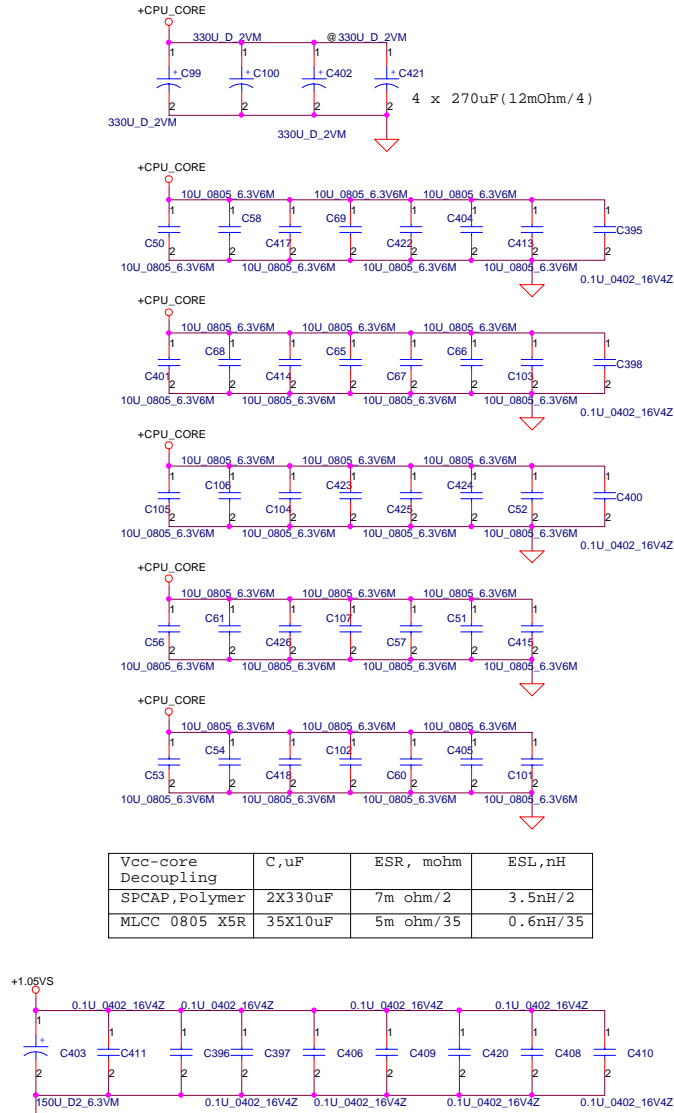
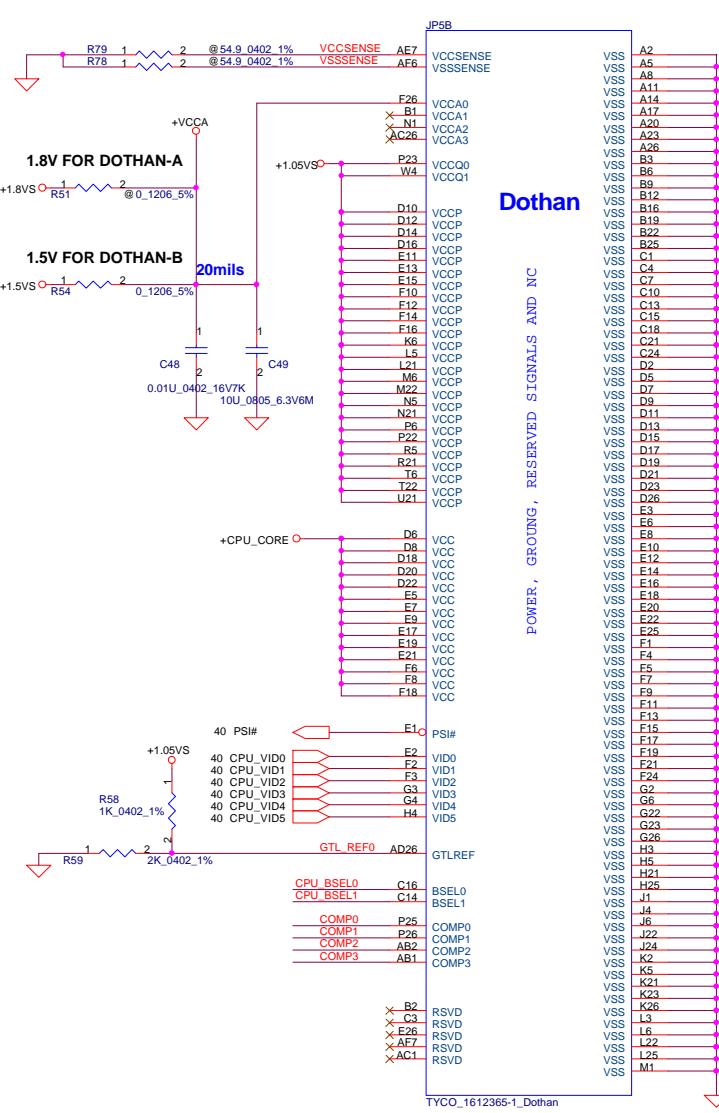
10E	SKU_ID	Board ID	Scan Code
1-Button		7	3
7-Buttons-W		5	2
7-Buttons-J		4	10
1-Button-J-HDD		3	11

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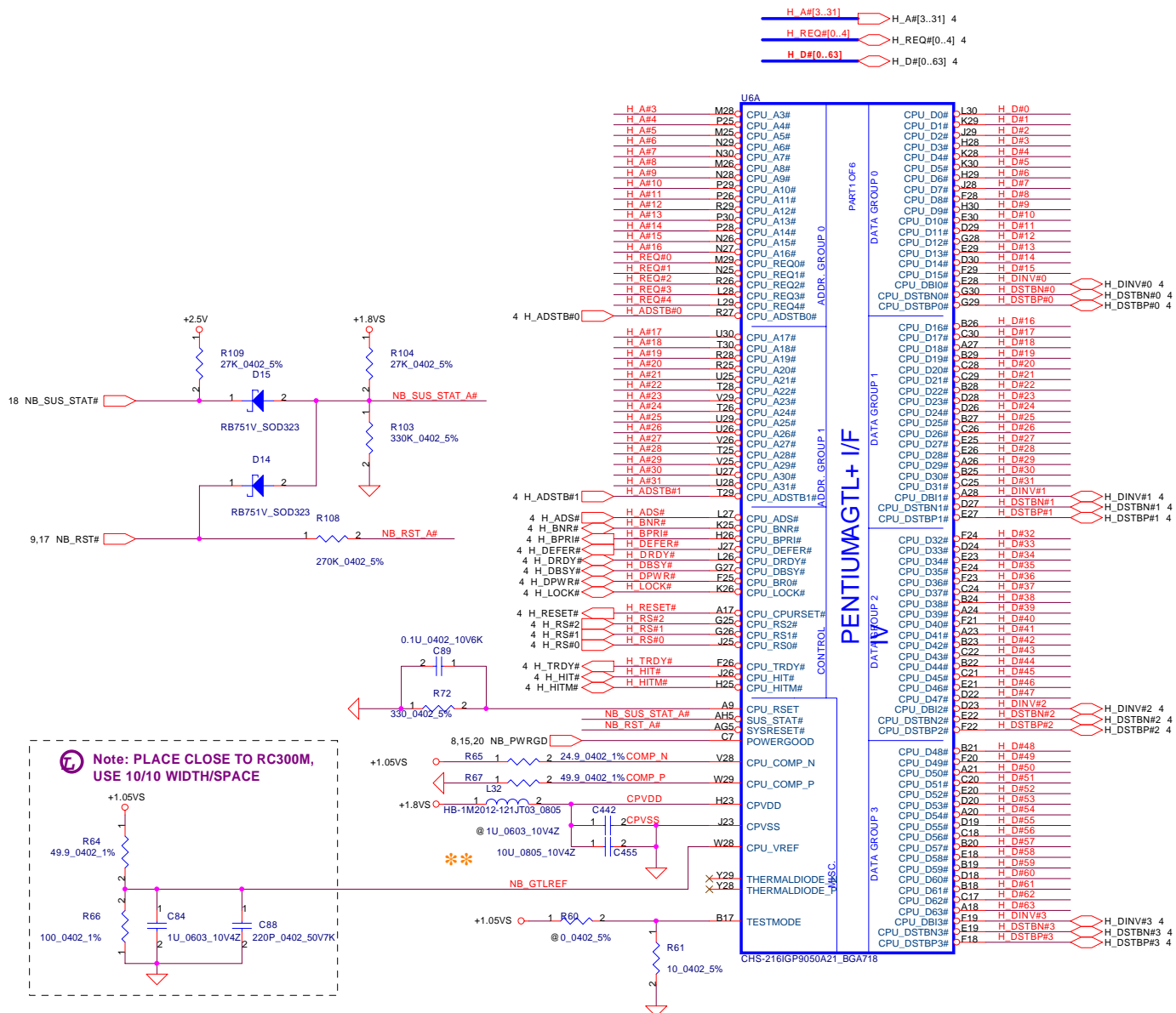
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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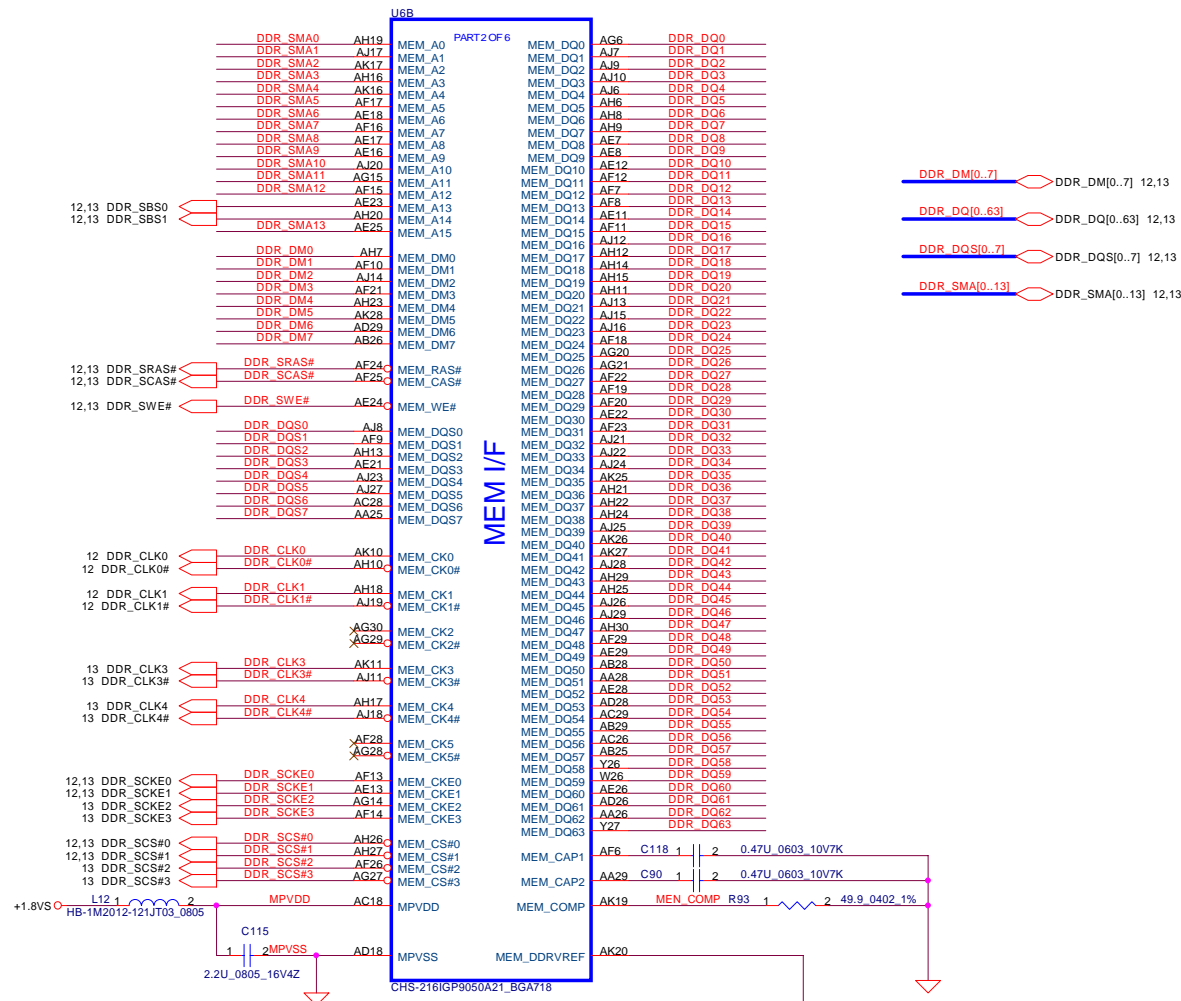
TRACE CLOSELY CPU < 0.5'
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 COMP1, COMP3 layout : Space 25mils

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U6A		PART1 OFB	
H_A#3 M28	CPU_A3#	CPU_D0# L30	H_D#0
H_A#4 P25	CPU_A4#	CPU_D1# K29	H_D#1
H_A#5 M25	CPU_A5#	CPU_D2# J29	H_D#2
H_A#6 N29	CPU_A6#	CPU_D3# H28	H_D#3
H_A#7 N30	CPU_A7#	CPU_D4# K28	H_D#4
H_A#8 M26	CPU_A8#	CPU_D5# K30	H_D#5
H_A#9 N28	CPU_A9#	CPU_D6# H29	H_D#6
H_A#10 P29	CPU_A10#	CPU_D7# J28	H_D#7
H_A#11 P26	CPU_A11#	CPU_D8# F28	H_D#8
H_A#12 R29	CPU_A12#	CPU_D9# H30	H_D#9
H_A#13 P30	CPU_A13#	CPU_D10# E30	H_D#10
H_A#14 P28	CPU_A14#	CPU_D11# Q29	H_D#11
H_A#15 N26	CPU_A15#	CPU_D12# G28	H_D#12
H_A#16 N27	CPU_A16#	CPU_D13# E29	H_D#13
H_REQ#0 M29	CPU_REQ0#	CPU_D14# D30	H_D#14
H_REQ#1 N25	CPU_REQ1#	CPU_D15# F29	H_D#15
H_REQ#2 R26	CPU_REQ2#	CPU_D16# E28	H_DINV#0
H_REQ#3 L28	CPU_REQ3#	CPU_D17# G30	H_DSTBN#0
H_REQ#4 L29	CPU_REQ4#	CPU_D18# G29	H_DSTBP#0
H_ADSTB#0 R27	CPU_ADSTB0#	CPU_D19# B26	H_D#16
H_A#17 U30	CPU_A17#	CPU_D20# C30	H_D#17
H_A#18 T30	CPU_A18#	CPU_D21# A27	H_D#18
H_A#19 R28	CPU_A19#	CPU_D22# B29	H_D#19
H_A#20 R25	CPU_A20#	CPU_D23# C28	H_D#20
H_A#21 U25	CPU_A21#	CPU_D24# C29	H_D#21
H_A#22 T28	CPU_A22#	CPU_D25# B28	H_D#22
H_A#23 V29	CPU_A23#	CPU_D26# D28	H_D#23
H_A#24 T28	CPU_A24#	CPU_D27# H27	H_D#24
H_A#25 U29	CPU_A25#	CPU_D28# B27	H_D#25
H_A#26 U26	CPU_A26#	CPU_D29# C26	H_D#26
H_A#27 V26	CPU_A27#	CPU_D30# E25	H_D#27
H_A#28 T25	CPU_A28#	CPU_D31# E26	H_D#28
H_A#29 V29	CPU_A29#	CPU_D32# B26	H_D#29
H_A#30 U27	CPU_A30#	CPU_D33# C25	H_D#30
H_A#31 U28	CPU_A31#	CPU_D34# A28	H_DINV#1
H_ADS# L27	CPU_ADS#	CPU_D35# D27	H_DSTBN#1
H_BNR# K25	CPU_BNR#	CPU_D36# E27	H_DSTBP#1
H_BPRI# H26	CPU_BPRI#	CPU_D37# F24	H_D#32
H_DEFER# J27	CPU_DEFER#	CPU_D38# D24	H_D#33
H_DRDY# L26	CPU_DRDY#	CPU_D39# E23	H_D#34
H_DBSY# G27	CPU_DBSY#	CPU_D40# E24	H_D#35
H_DPWR# F25	CPU_DPWR#	CPU_D41# E24	H_D#36
H_LOCK# K26	CPU_LOCK#	CPU_D42# C24	H_D#37
H_RESET# A17	CPU_RESET#	CPU_D43# B24	H_D#38
H_RS#2 G25	CPU_RS2#	CPU_D44# A24	H_D#39
H_RS#1 G26	CPU_RS1#	CPU_D45# A23	H_D#40
H_RS#0 J25	CPU_RS0#	CPU_D46# B23	H_D#41
H_TRDY# F26	CPU_TRDY#	CPU_D47# C22	H_D#42
H_HIT# J26	CPU_HIT#	CPU_D48# C22	H_D#43
H_HITM# H25	CPU_HITM#	CPU_D49# B22	H_D#44
A9	CPU_RSET	CPU_D50# D22	H_D#45
AH5	SUS_STAT#	CPU_D51# E21	H_D#46
AG5	SUS_STAT#	CPU_D52# D22	H_D#47
C7	SYRSET#	CPU_D53# D23	H_DINV#2
V28	CPU_COMP_N	CPU_D54# E22	H_DSTBN#2
W29	CPU_COMP_P	CPU_D55# E22	H_DSTBP#2
H23	CPVDD	CPU_D56# B21	H_D#48
J23	CPVSS	CPU_D57# F20	H_D#49
W28	CPU_VREF	CPU_D58# A21	H_D#50
X29	THERMALDIODE_P	CPU_D59# C20	H_D#51
X28	THERMALDIODE_N	CPU_D60# E20	H_D#52
B17	TESTMODE	CPU_D61# D20	H_D#53
		CPU_D62# A20	H_D#54
		CPU_D63# D19	H_D#55
		CPU_D64# C18	H_D#56
		CPU_D65# B20	H_D#57
		CPU_D66# H19	H_D#58
		CPU_D67# B18	H_D#59
		CPU_D68# B19	H_D#60
		CPU_D69# C17	H_D#61
		CPU_D70# C17	H_D#62
		CPU_D71# A18	H_D#63
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		CPU_D73# E19	H_DSTBN#3
		CPU_D74# E18	H_DSTBP#3

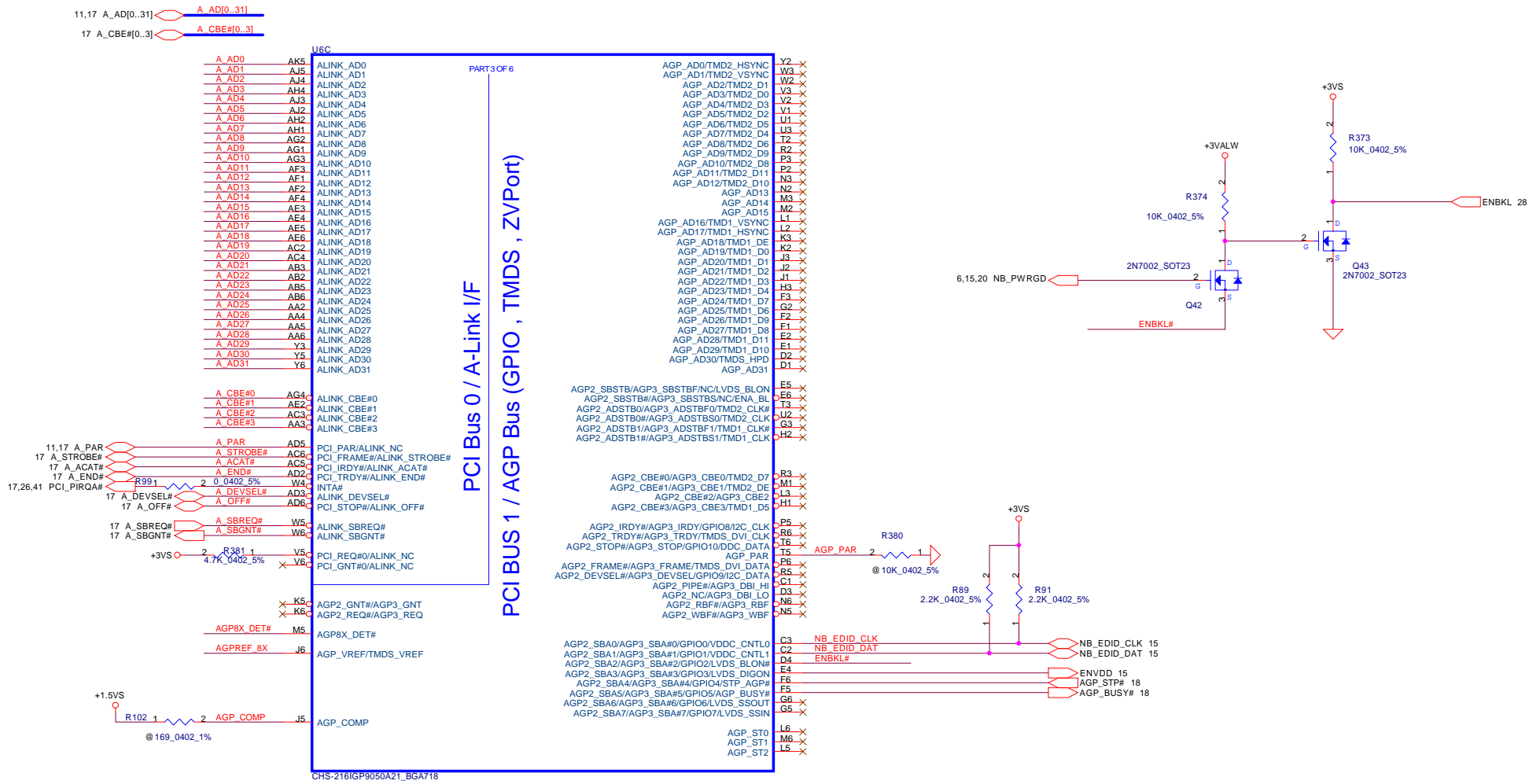
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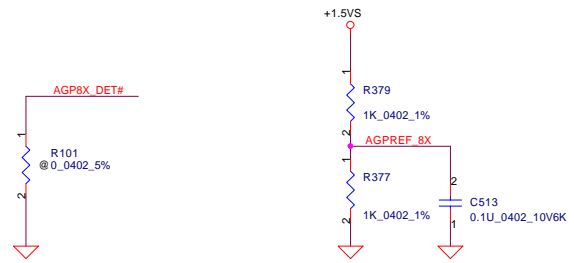
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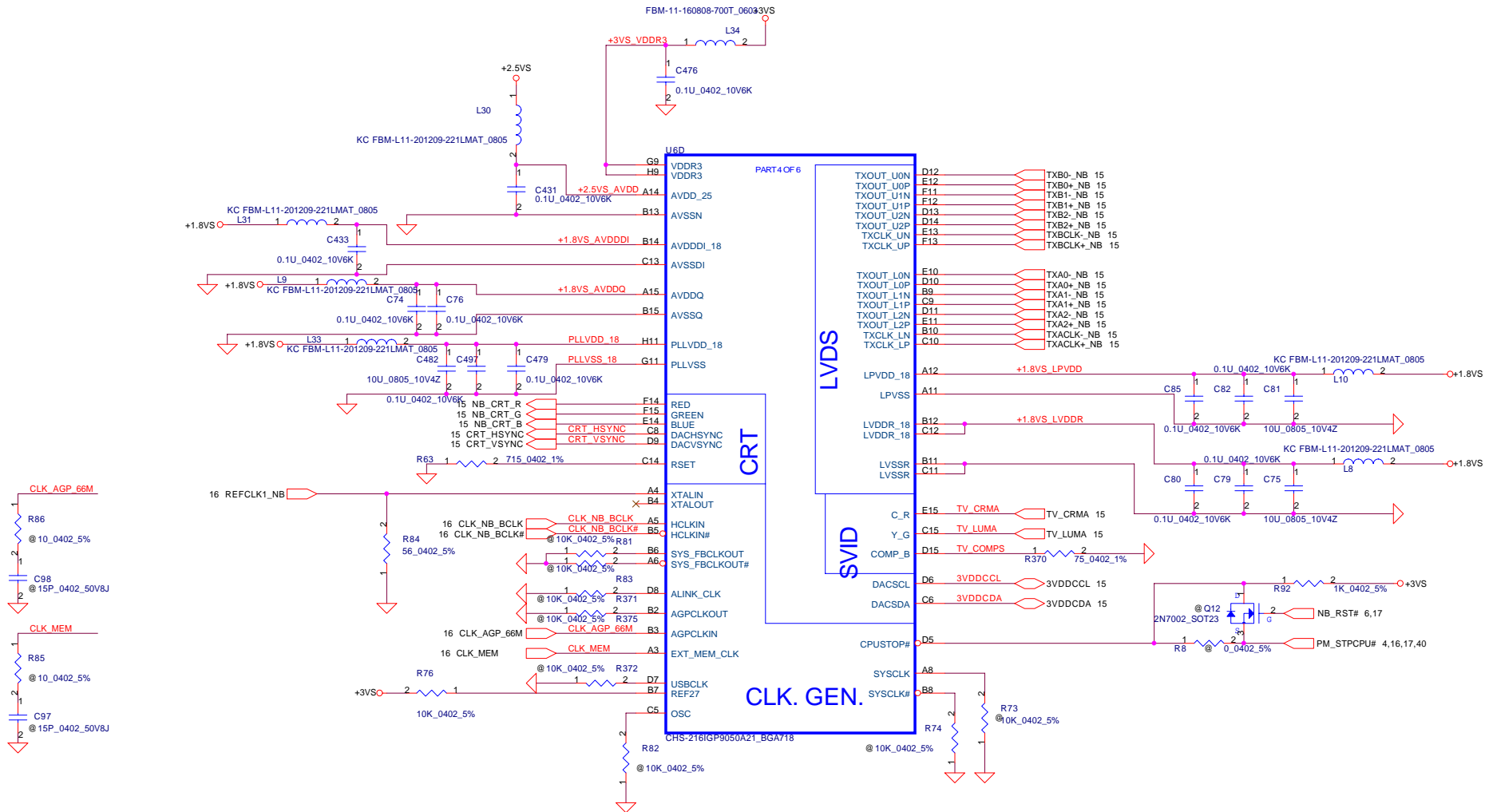
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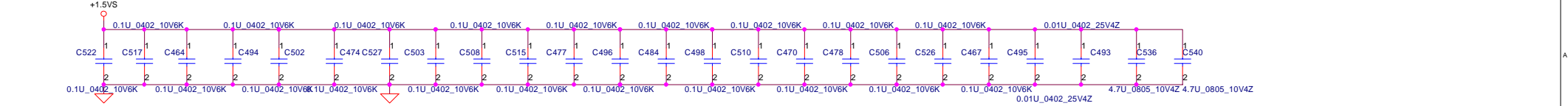
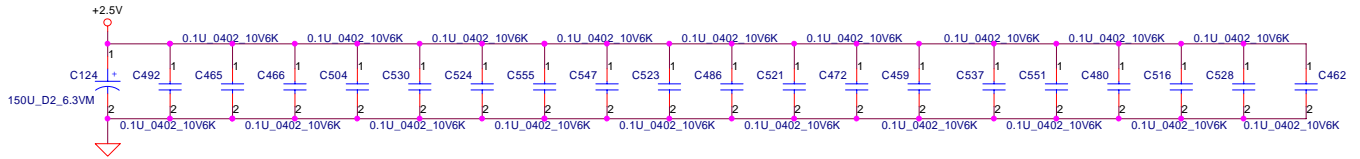
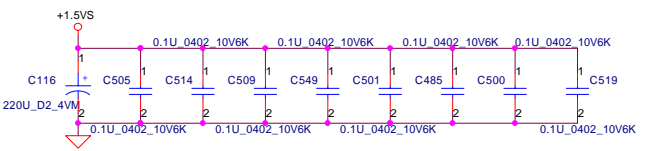
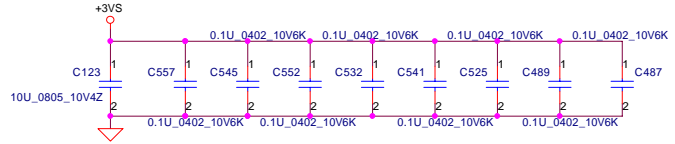
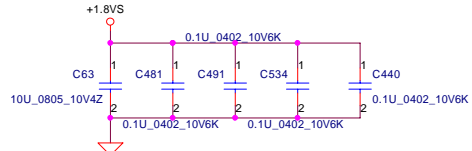
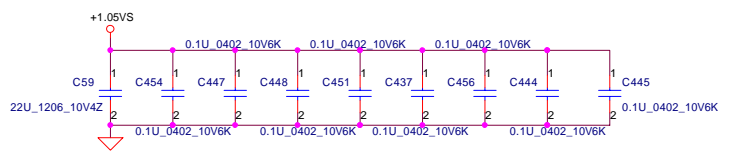
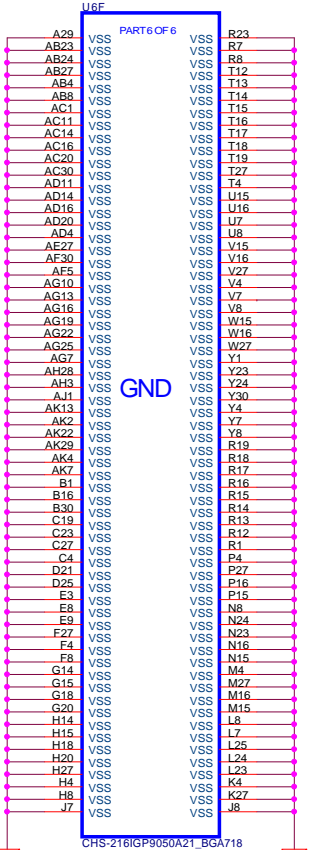
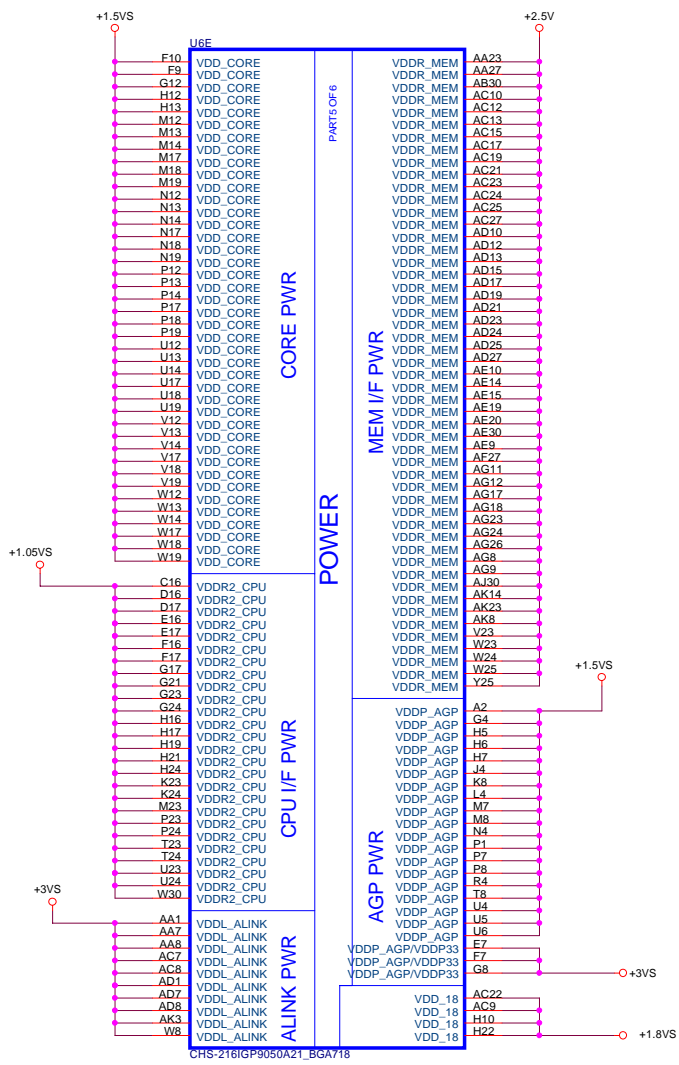
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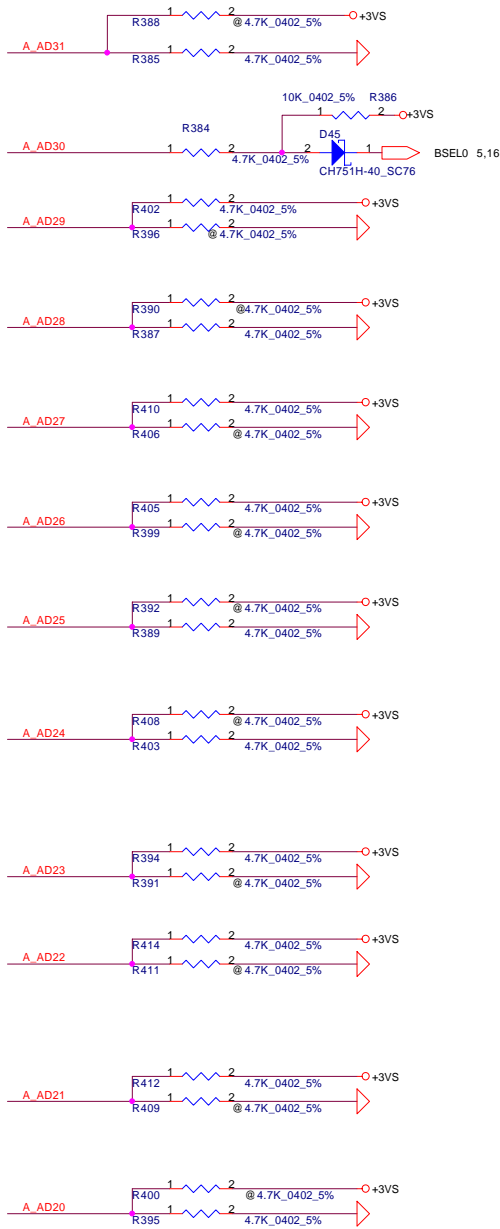
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8.17 A_AD[0..31] ◊ A_AD[0..31]

A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01

- 00: 100 MHZ
- 01: 133 MHZ
- 10: 200MHZ
- 11:166 MHZ

A_AD29: STRAP CONFIGURATION

DEFAULT:1

- 0: REDUCEDE SET
- 1: FULL SET

A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0

- 0: DISABLE
- 1: ENABLE

A_AD27: FrcShortReset#

DEFAULT: 1

- 0: TEST MODE
- 1: NORMAL MODE

A_AD26 : ENABLE IOQ

DEFAULT: 1

- 0: IOQ=1
- 1: IOQ=12

A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10

- 00: 1.05V
- 01: 1.35V
- 11: 1.75V
- 10: 1.45V

A_AD24 : MOBILE CPU SELECT

DEFAULT: 1

- 0: BANIAS CPU
- 1: OTHER CPU

A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1

- 0: TEST MODE
- 1: NORMAL

A_AD22 : OSC PAD OUTPUT PCICLK

DEFAULT : 1

- 0: PCICLK OUT
- 1: OSC CLK OUT

A_AD21 : AUTO_CAL ENABLE

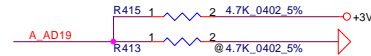
DEFAULT : 1

- 0: DISABLE
- 1: ENABLE

A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0

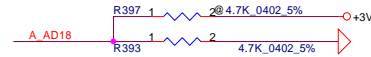
- 0: DISABLE
- 1: ENABLE



A_AD19 : MEMORY IO VOLTAGE

DEFAULT: 1

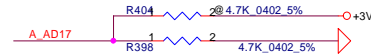
- 0: 1.8V
- 1: 2.5V



A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0

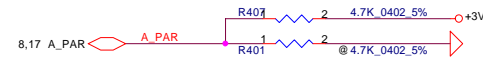
- 0: DISABLE
- 1:ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0

- 00: 1.05V
- 01: 1.35V
- 11: 1.75V
- 10: 1.45V

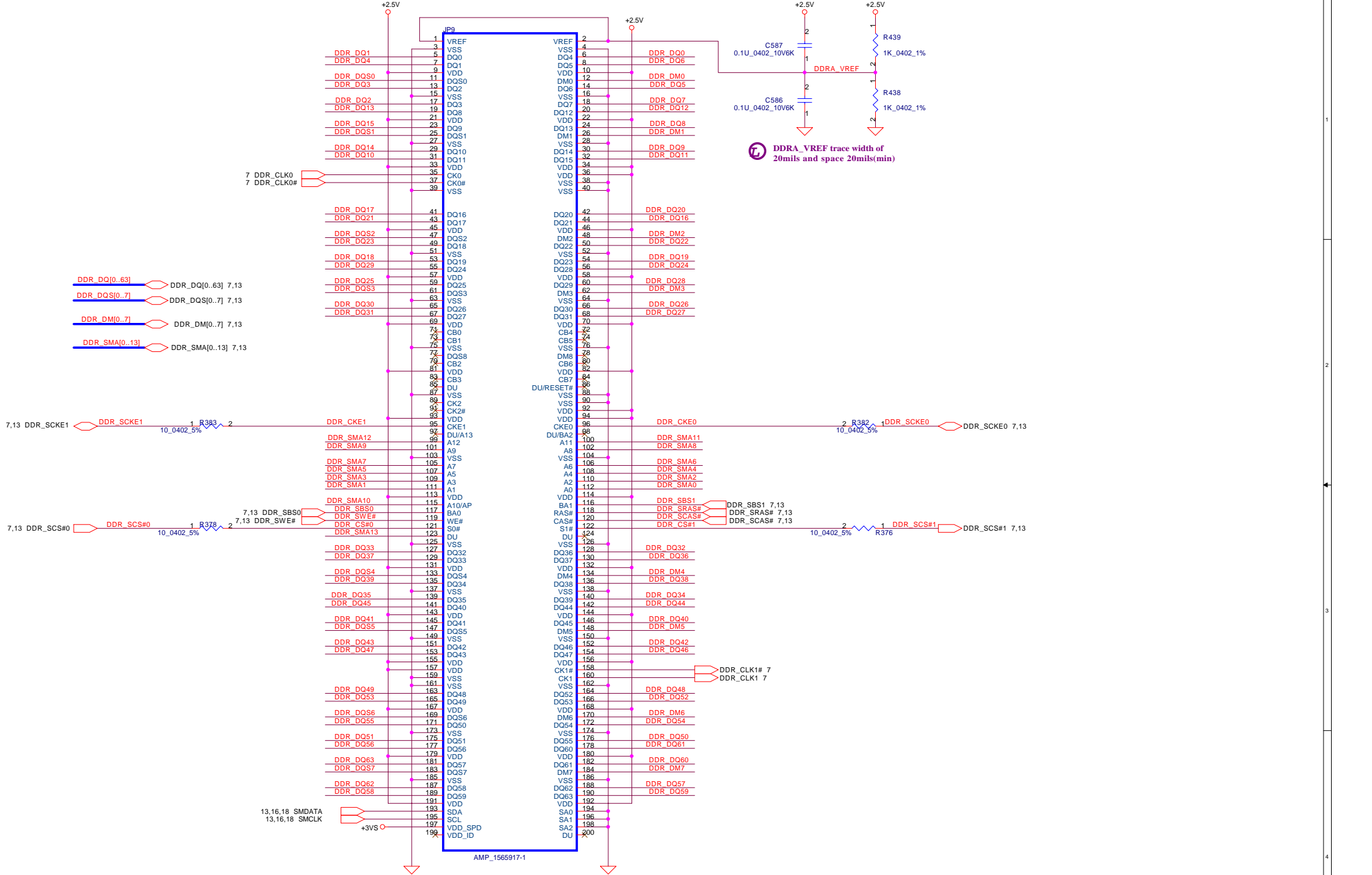


PAR: EXTENDED DEBUG MODE

DEFAULT : 1

- 0: DEBUG MODE
- 1: NORMAL

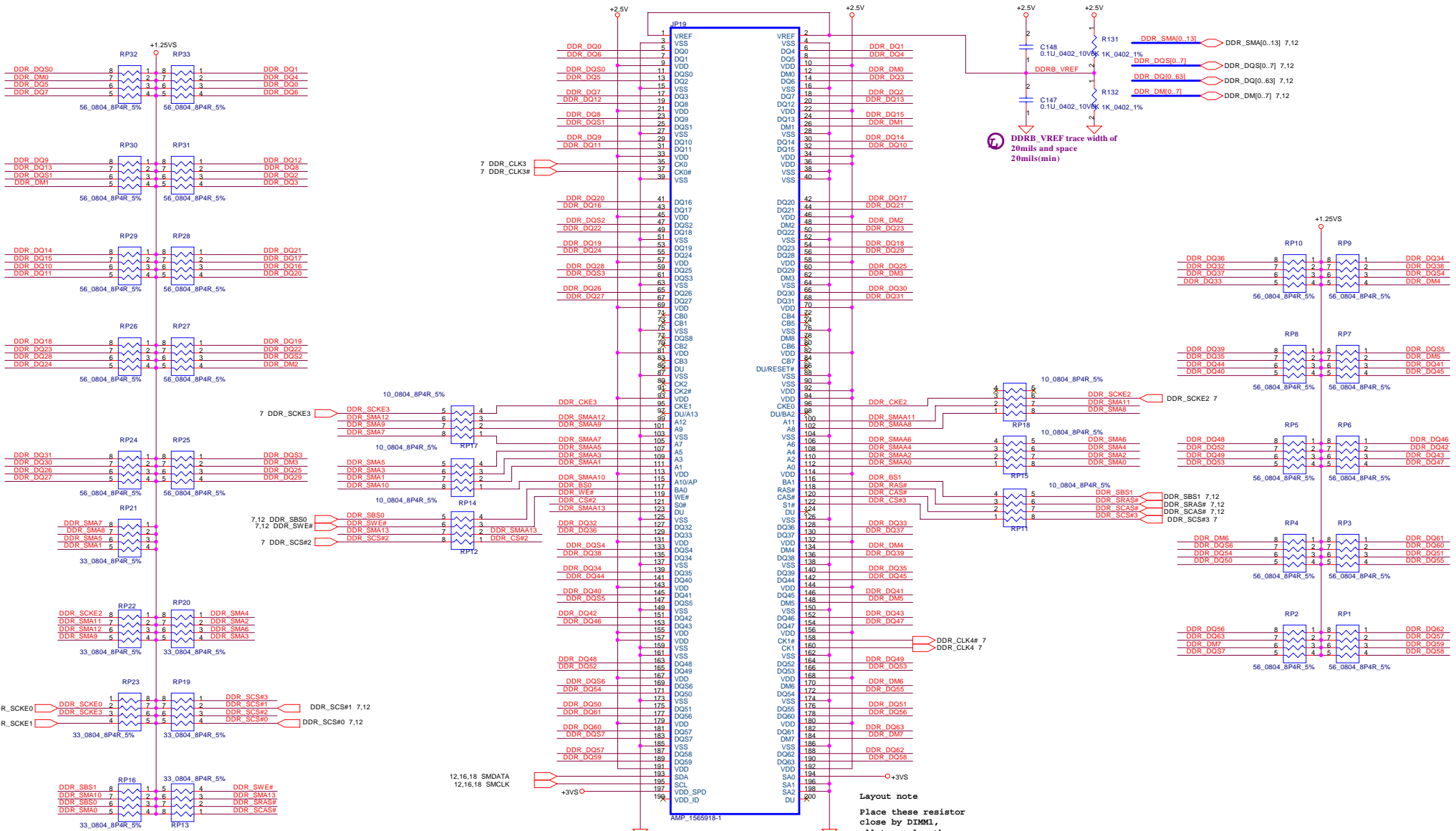
Security Classification	Compal Secret Data			Title
Issued Date	2005/03/01	Deciphered Date	2006/03/01	ATI RL300MB-SYSTEM STRAP
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				Document Number Sakhir 10E-HBT10>
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Layout note

Layout note
Place Add/Command resistors
close to Pin, max L = 300 mils

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				Custom	Sakhr 10E-HBT10>
				Rev	1.0
Date: 星期三, 五月 04, 2005				Sheet	12 of 44

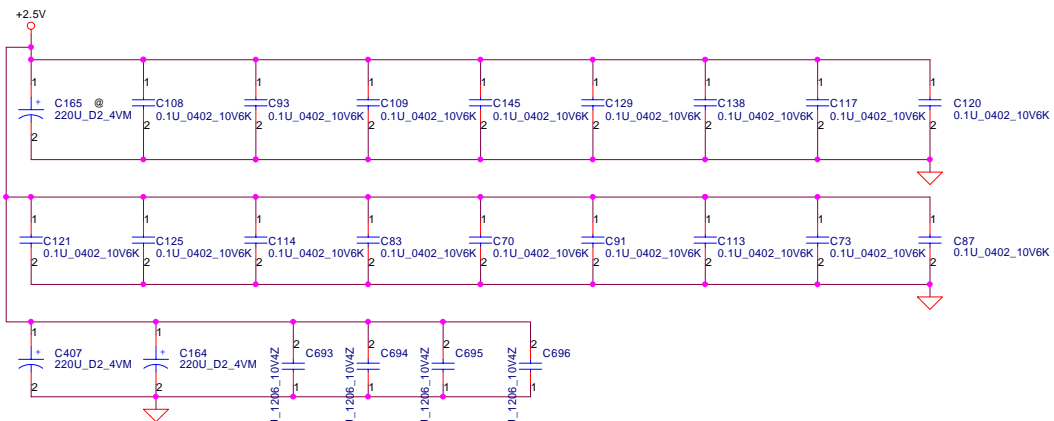


DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

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Issued Date	2005/03/01	Deciphered Date	2006/03/01
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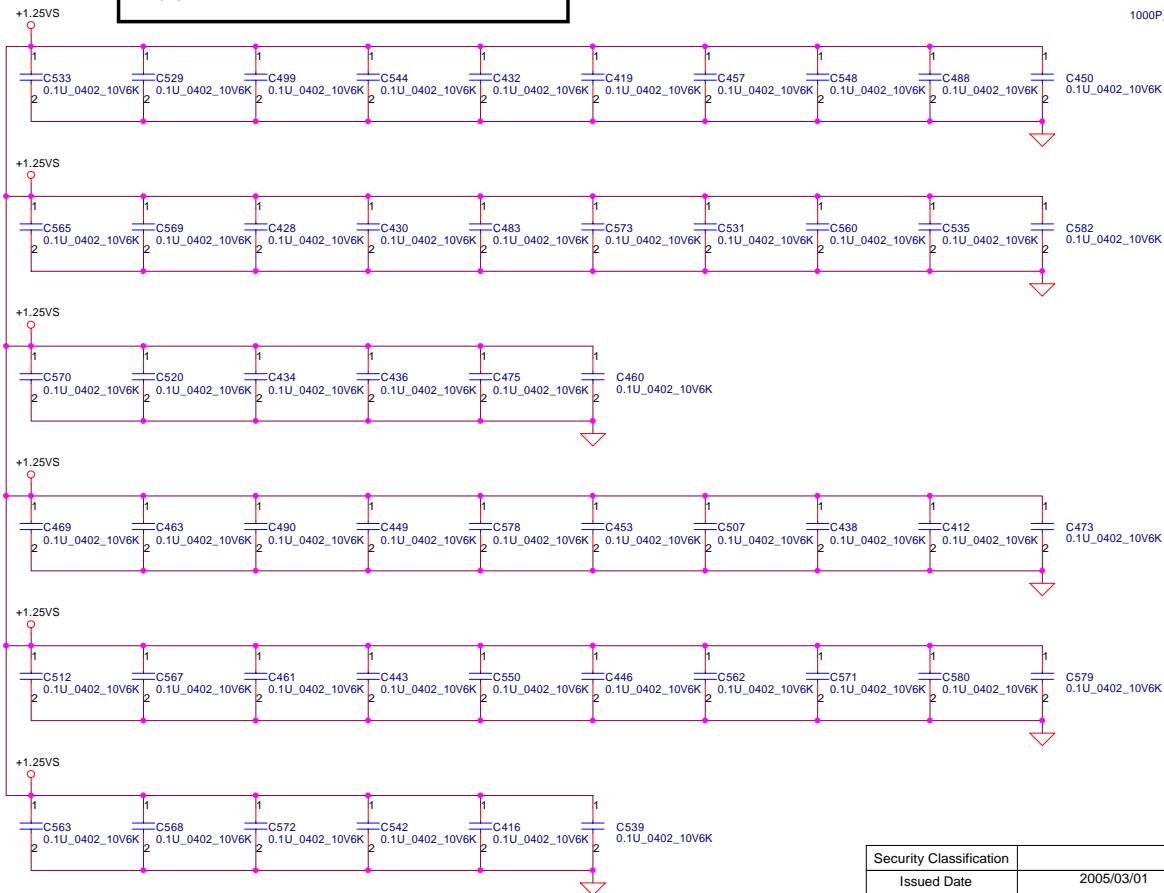
Layout note :

Distribute as close as possible to DDR-SODIMM0.



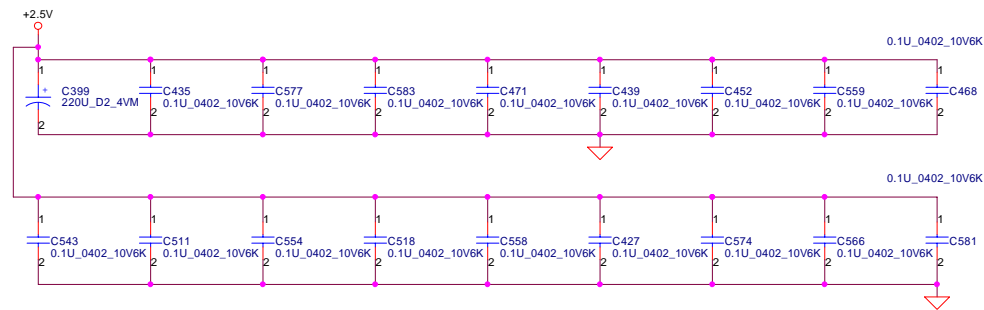
Layout note :

Place one cap close to every 2 pull up resistors termination to +1.25VS



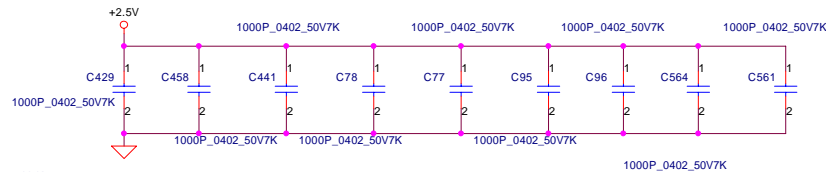
Layout note :

Distribute as close as possible to DDR-SODIMM1.

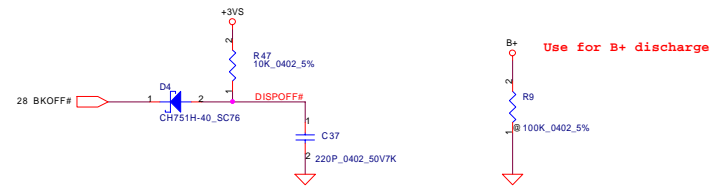
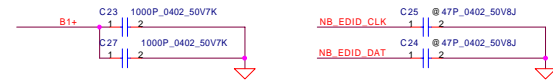
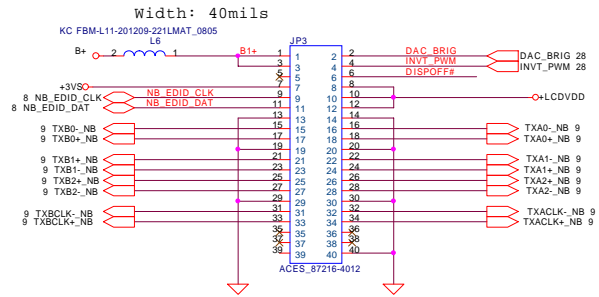
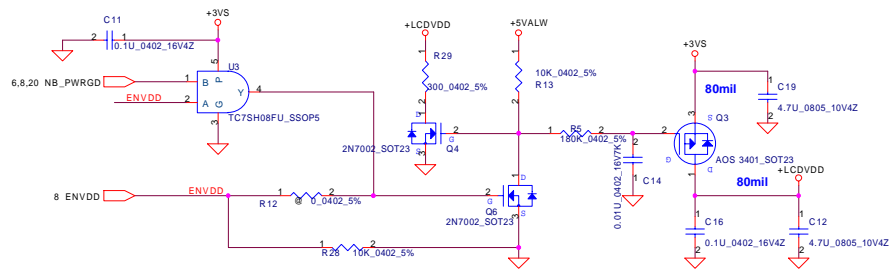


Layout note :

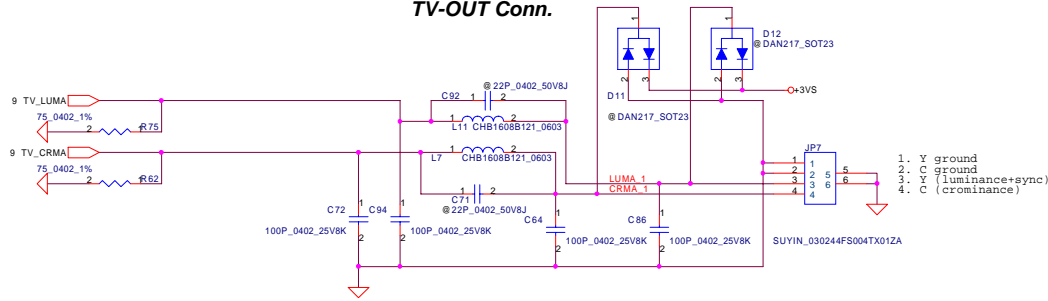
for EMI solution



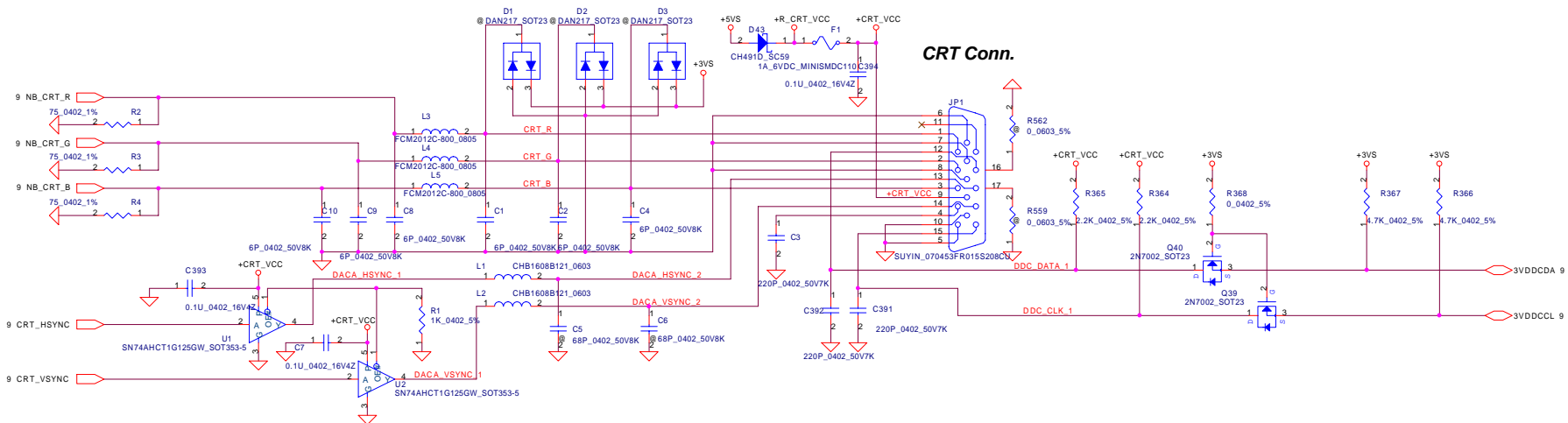
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	DDR SODIMM Decoupling	
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Customer	Sakhir 10E-HBT10>			10E	1.0
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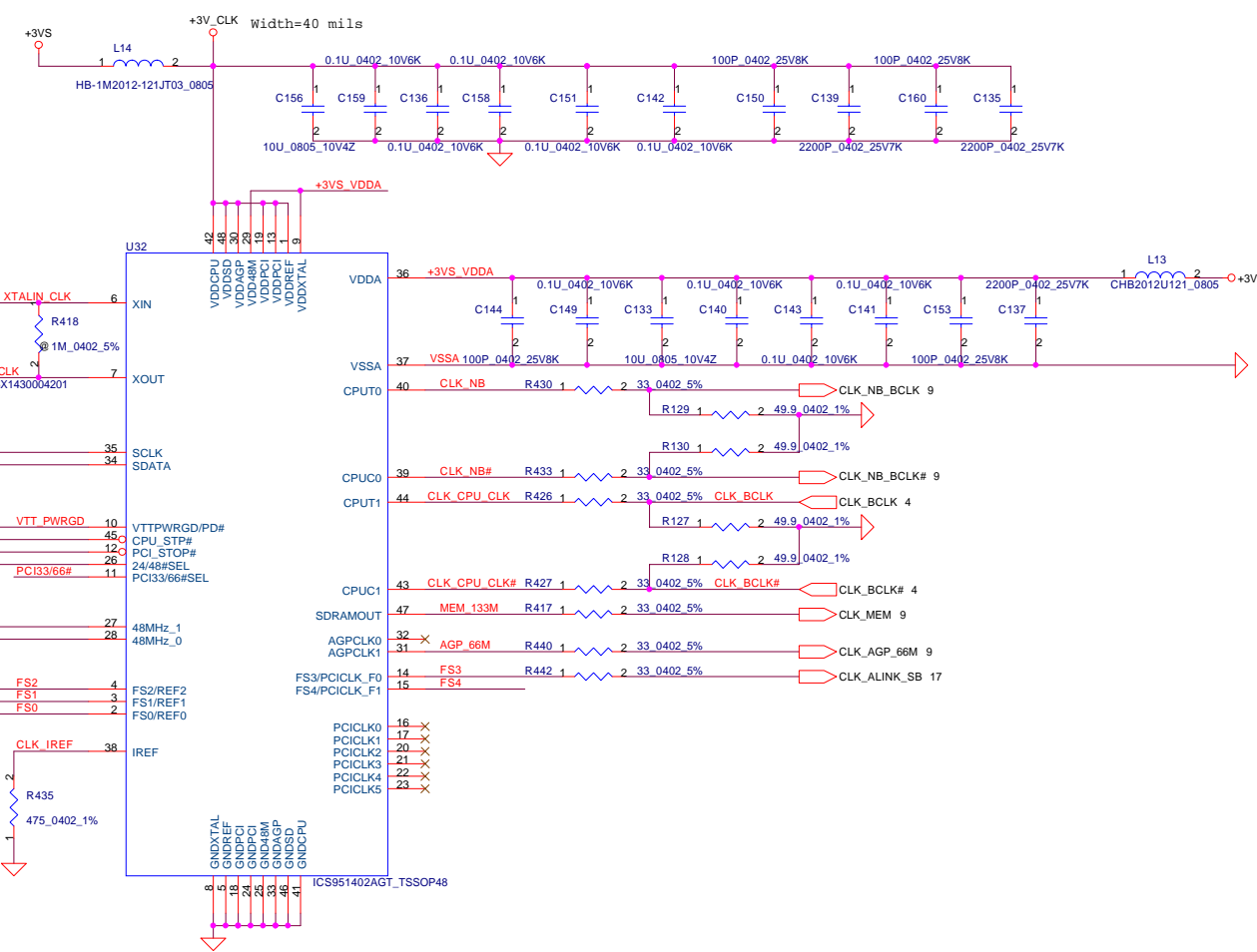
TV-OUT Conn.



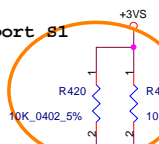
CRT Conn.



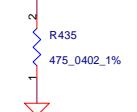
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Unpop when support S1



Pop when using LPC debug card

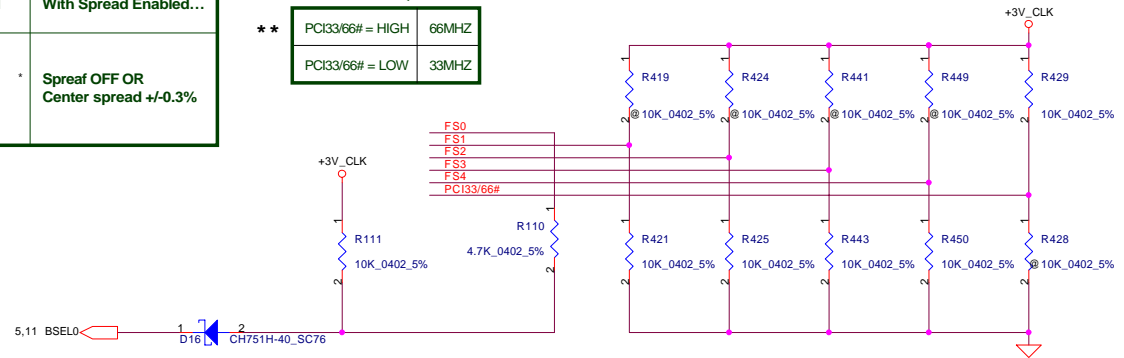


CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	
0	0	0	0	1	133	133	Spread OFF OR Center spread +/-0.3%
0	0	0	0	0	100	100	

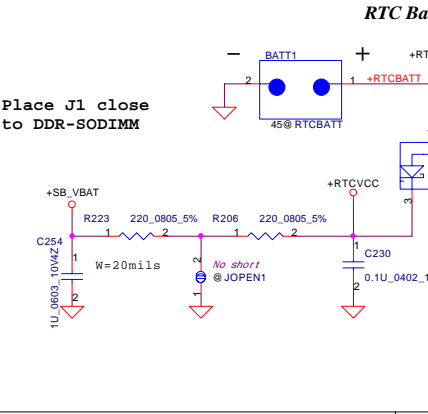
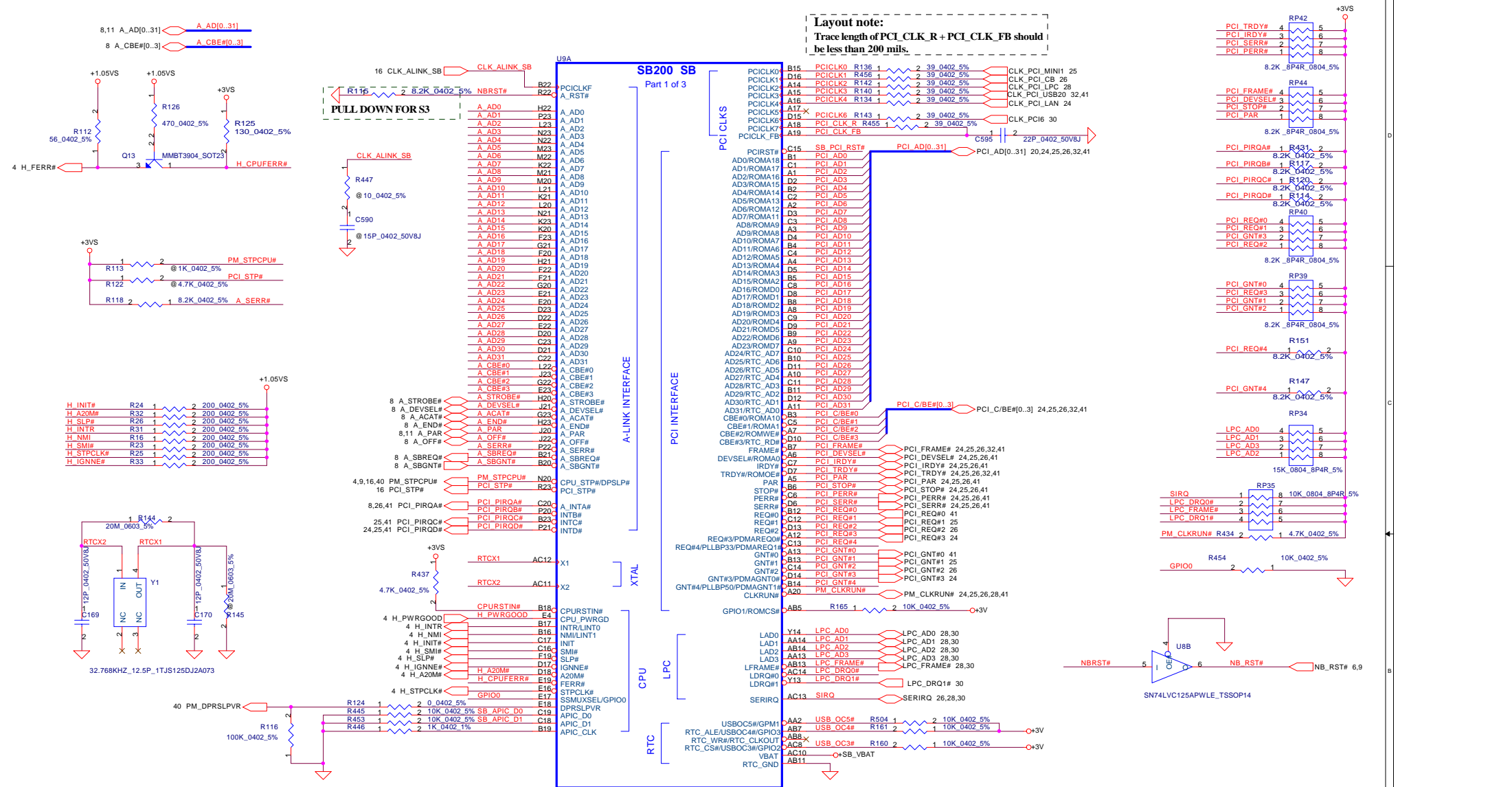
A-LINK FREQ

PC133/66# = HIGH	66MHZ
PC133/66# = LOW	33MHZ

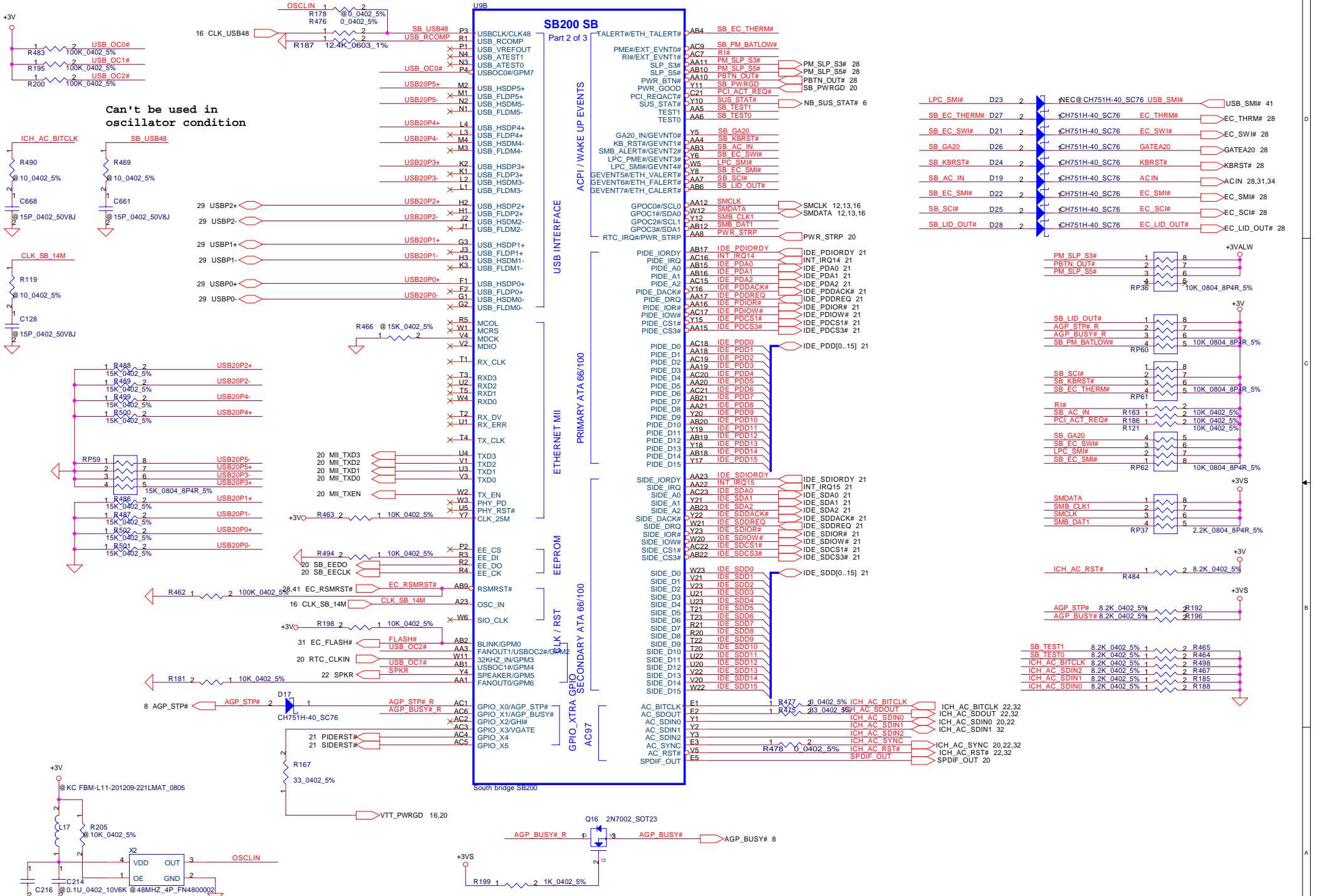


Note: 0 = PULL LOW
1 = PULL HIGH

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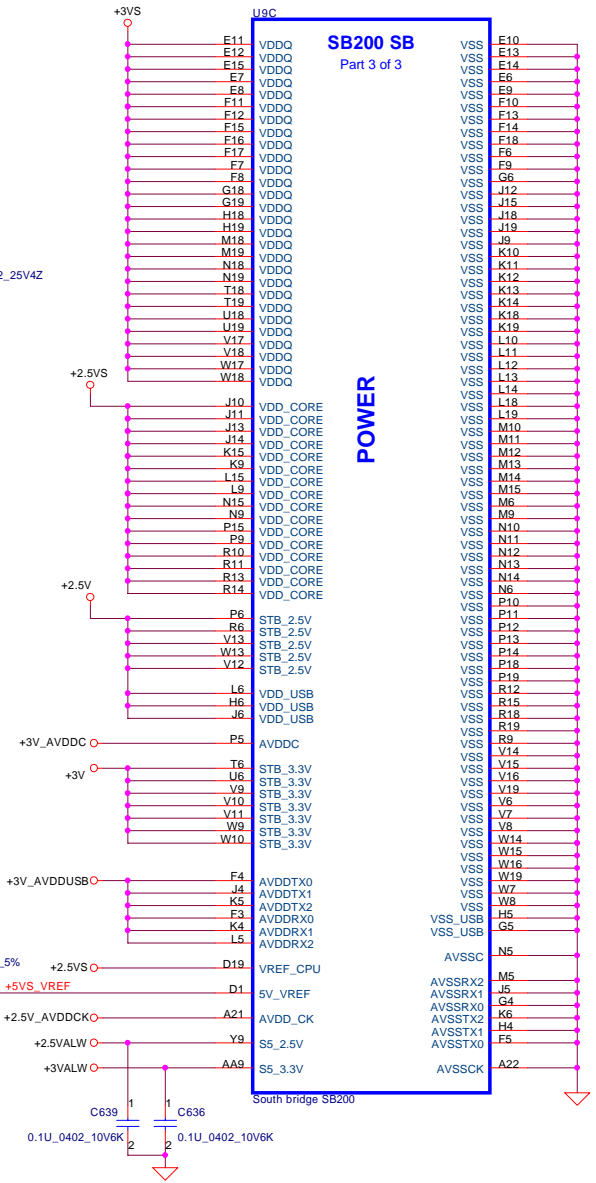
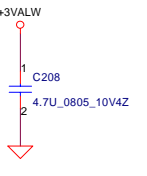
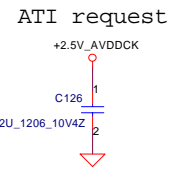
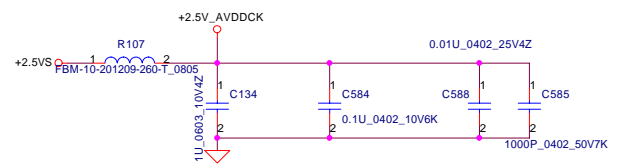
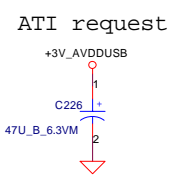
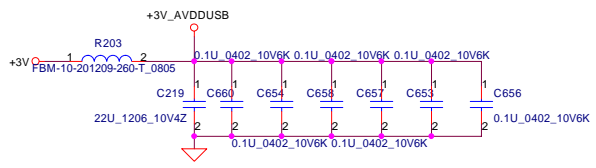
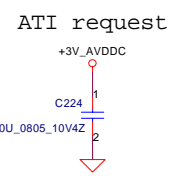
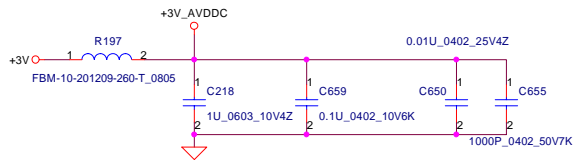
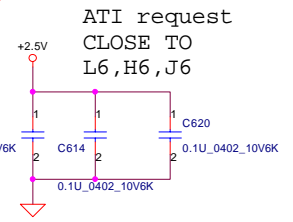
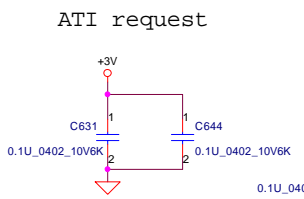
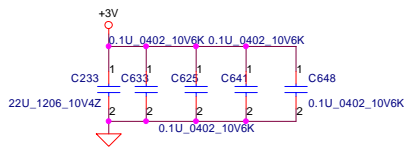
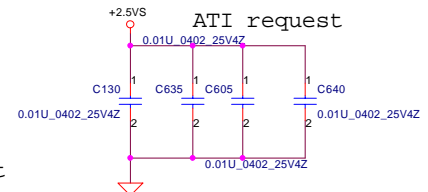
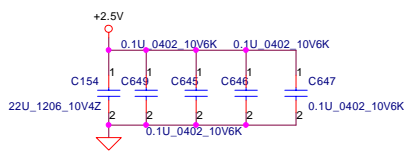
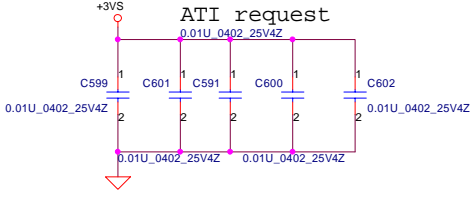
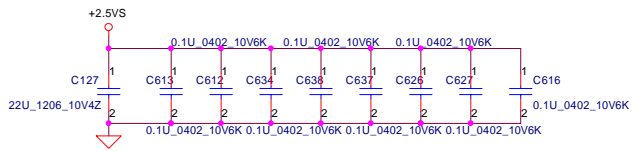
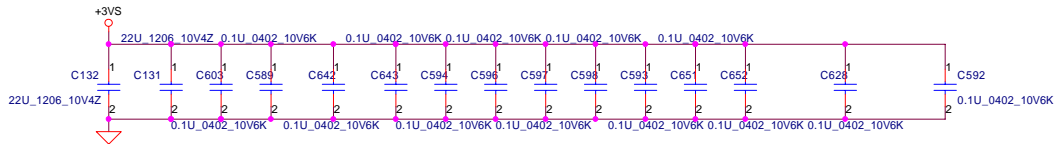


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Date:	星期三, 五月 04, 2005	Sheet	17	of	44
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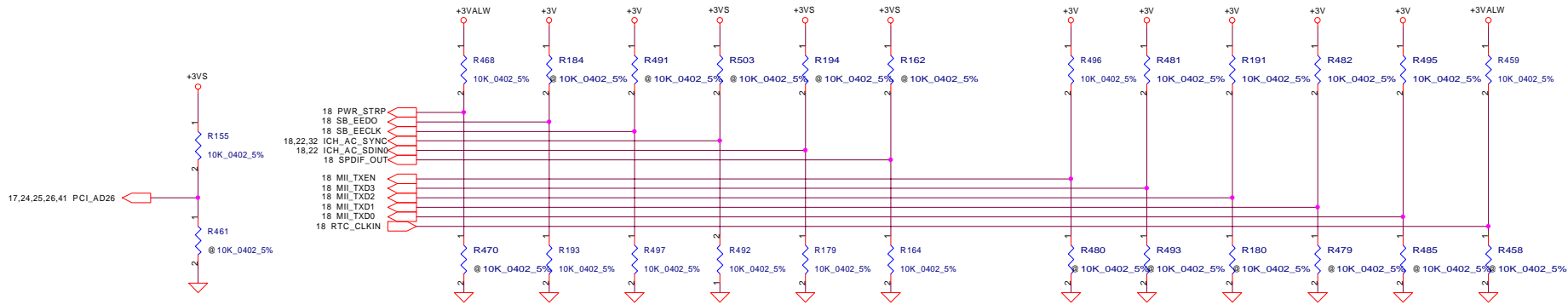
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Issued Date	2005/03/01	Deciphered Date
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Title		
SB200M(2/4) - IDE/USB/MII		
Size	Document Number	Rev
Custom	Sakhir 10E-HBT10>	1.0
Date:	星期三, 五月 04, 2005	Sheet 18 of 44



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Title		
SB200M(3/4) - PWR		
Size	Document Number	Rev
Custom	Sakhir 10E+HBT10>	1.0
Date	星期三, 五月 04, 2005	Sheet 19 of 44

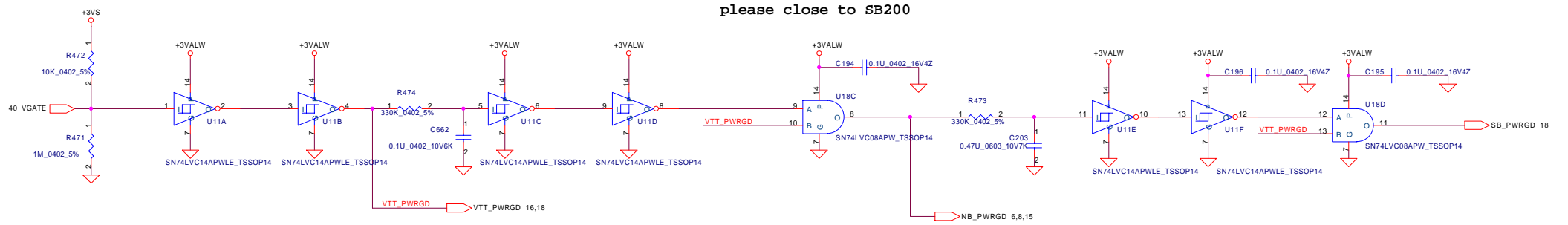


PCI_AD26 H: ENE910
L: NS87591

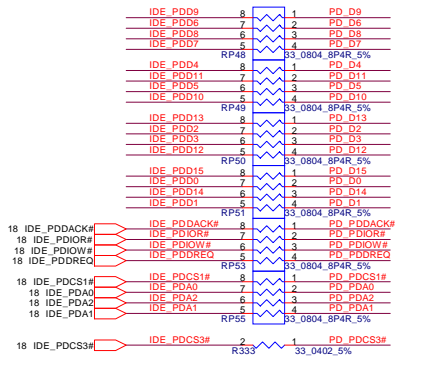
REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	IAC_SYNC	IAC_SDAT0A	SPDIF_OUT	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ S5 RTC_CLKIN
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)

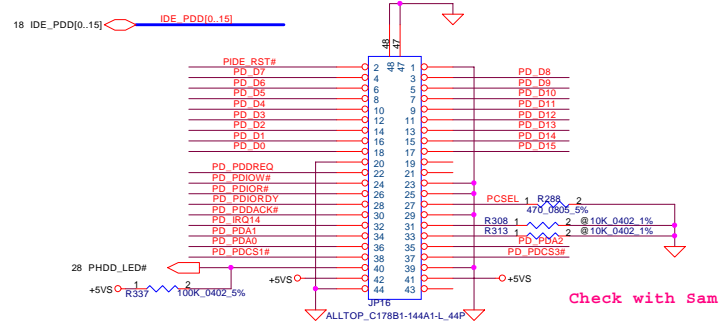
please close to SB200



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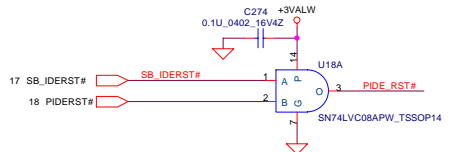


HDD CONNECTOR

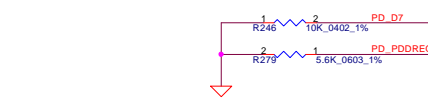
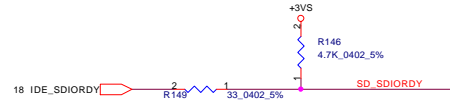
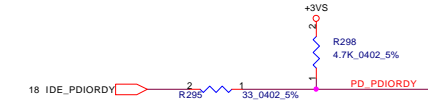
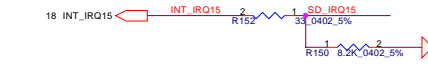
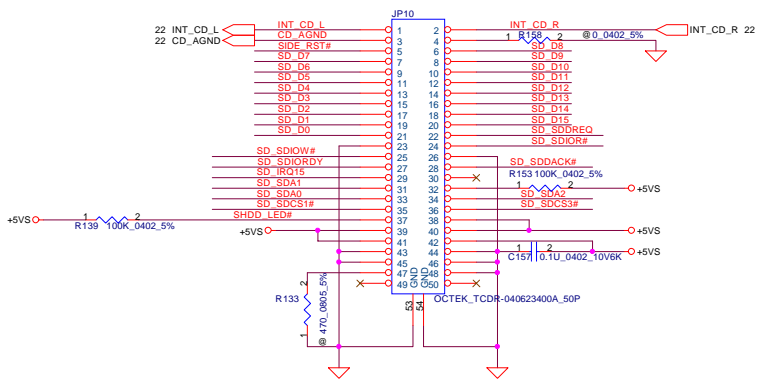
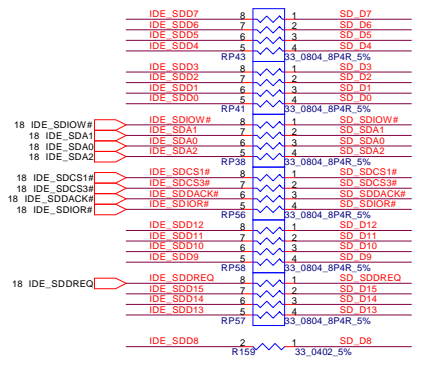
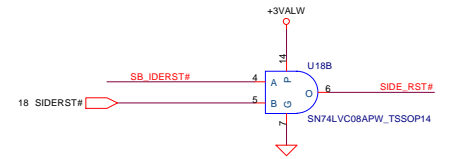


Check with Sam

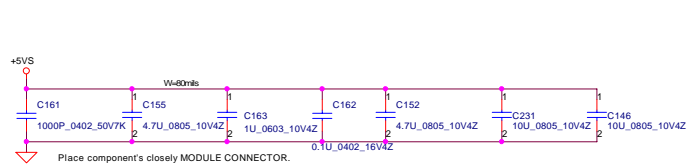
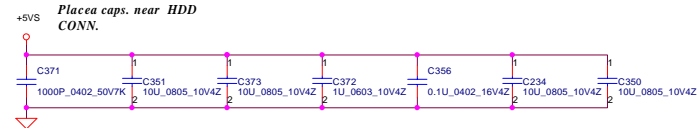
Check with ME new connector and Pin 1



Place U11 near SB side

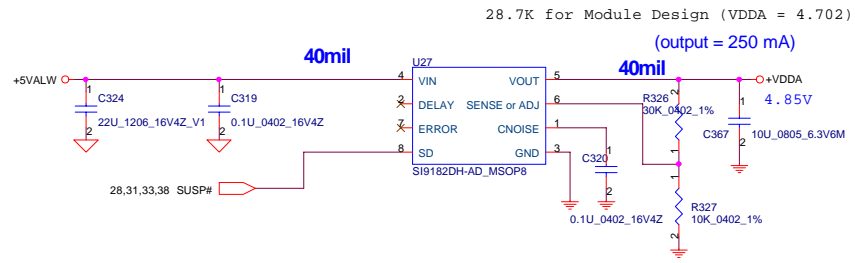
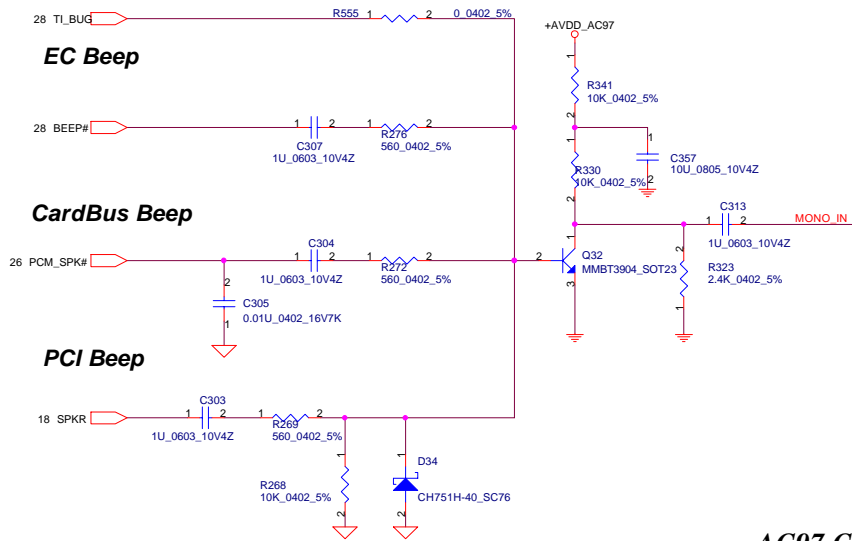


Should place close to SB side

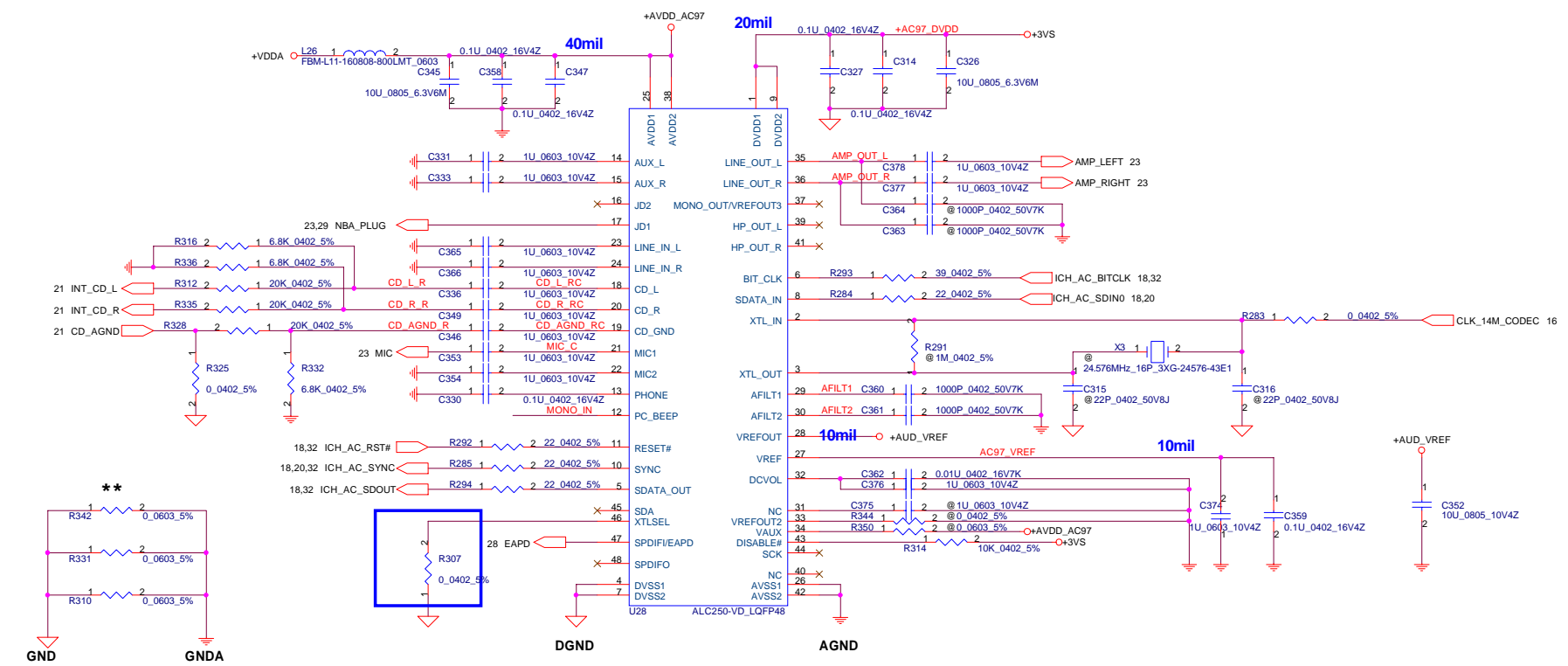


Place components closely MODULE CONNECTOR.

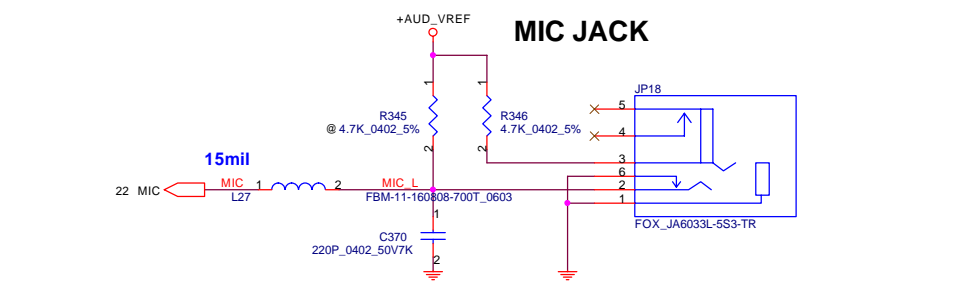
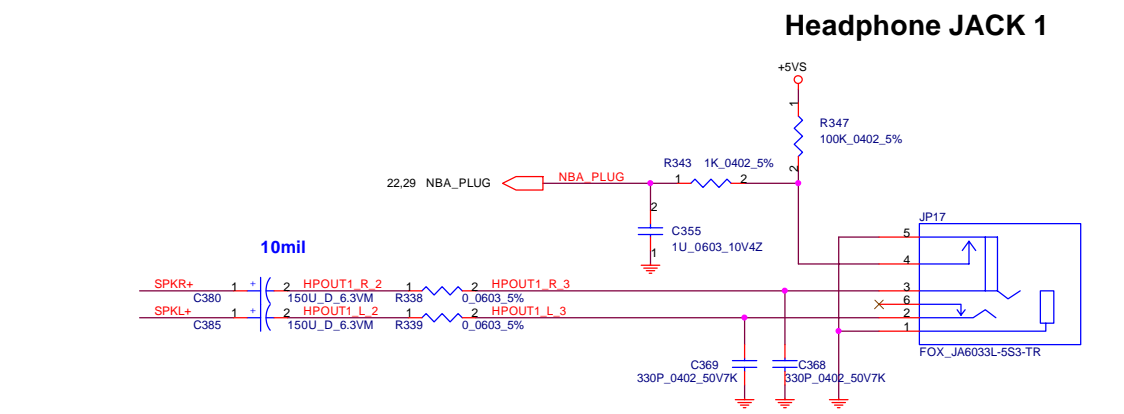
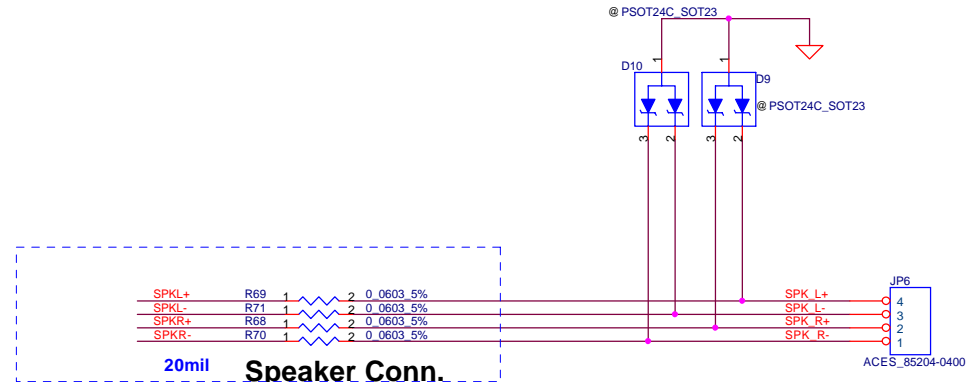
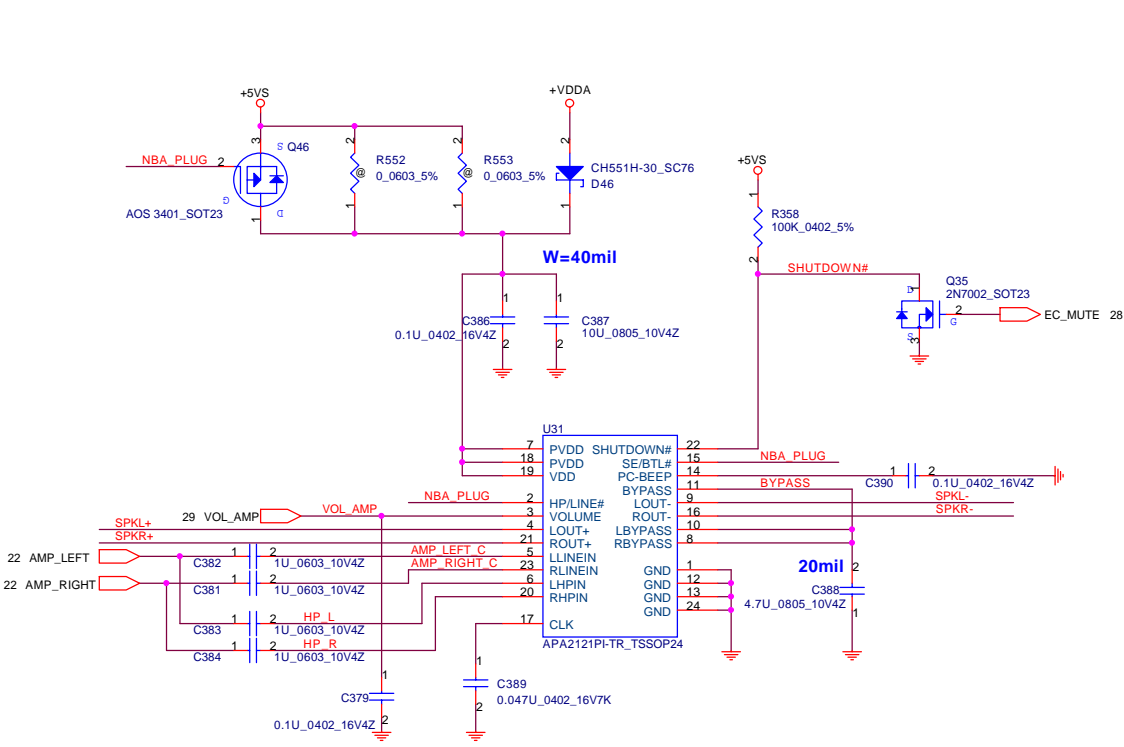
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/01	Deciphered Date	2006/03/01	IDE/ FDD MODULE CONN.	
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AC97 Codec



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				Customer	Sakhr 10E-HBT10>
				Date	星期三, 五月 04, 2005
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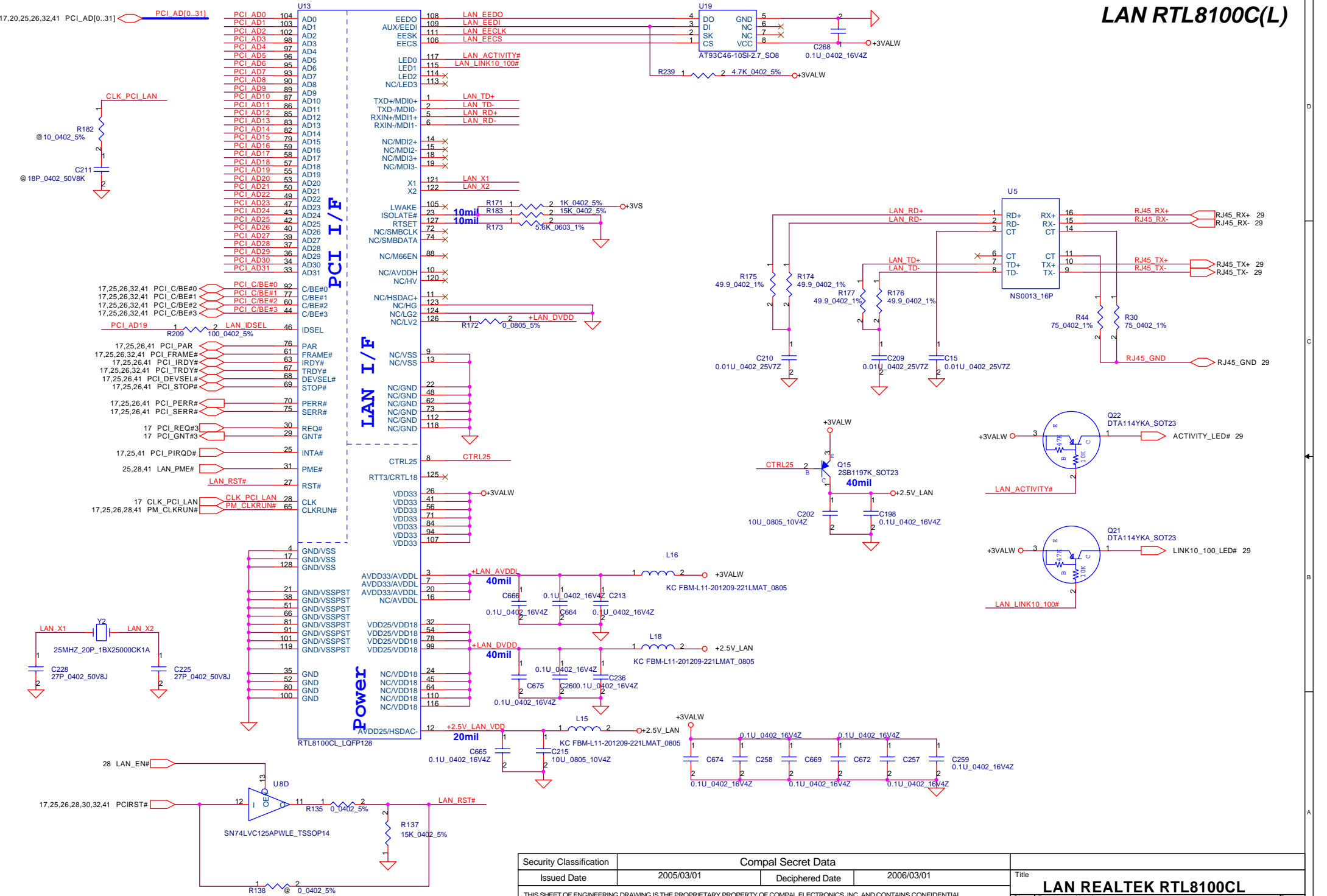


Headphone JACK 1

MIC JACK

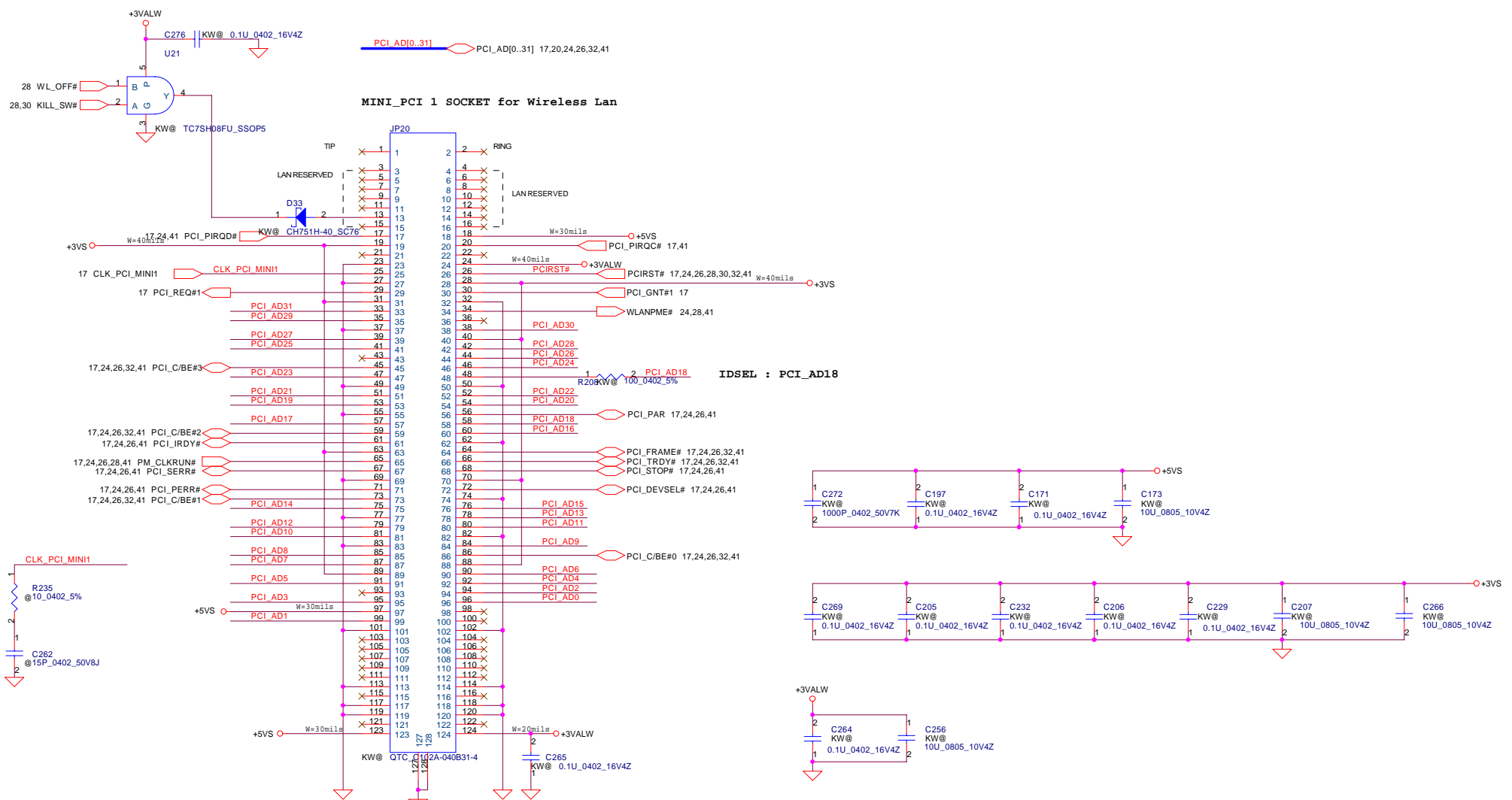
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LAN RTL8100C(L)

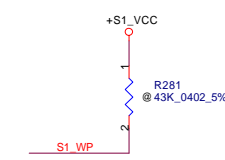
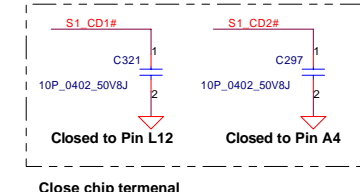
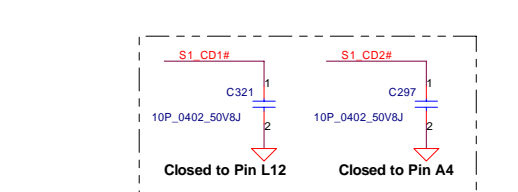
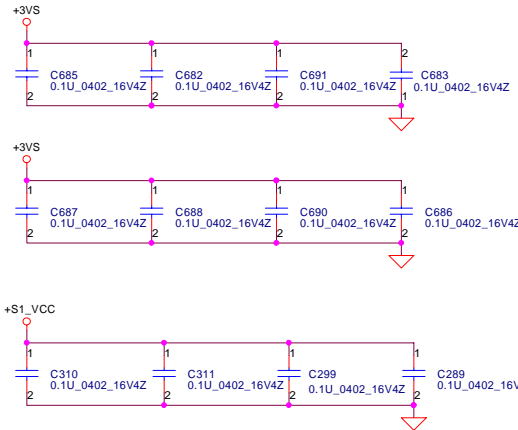
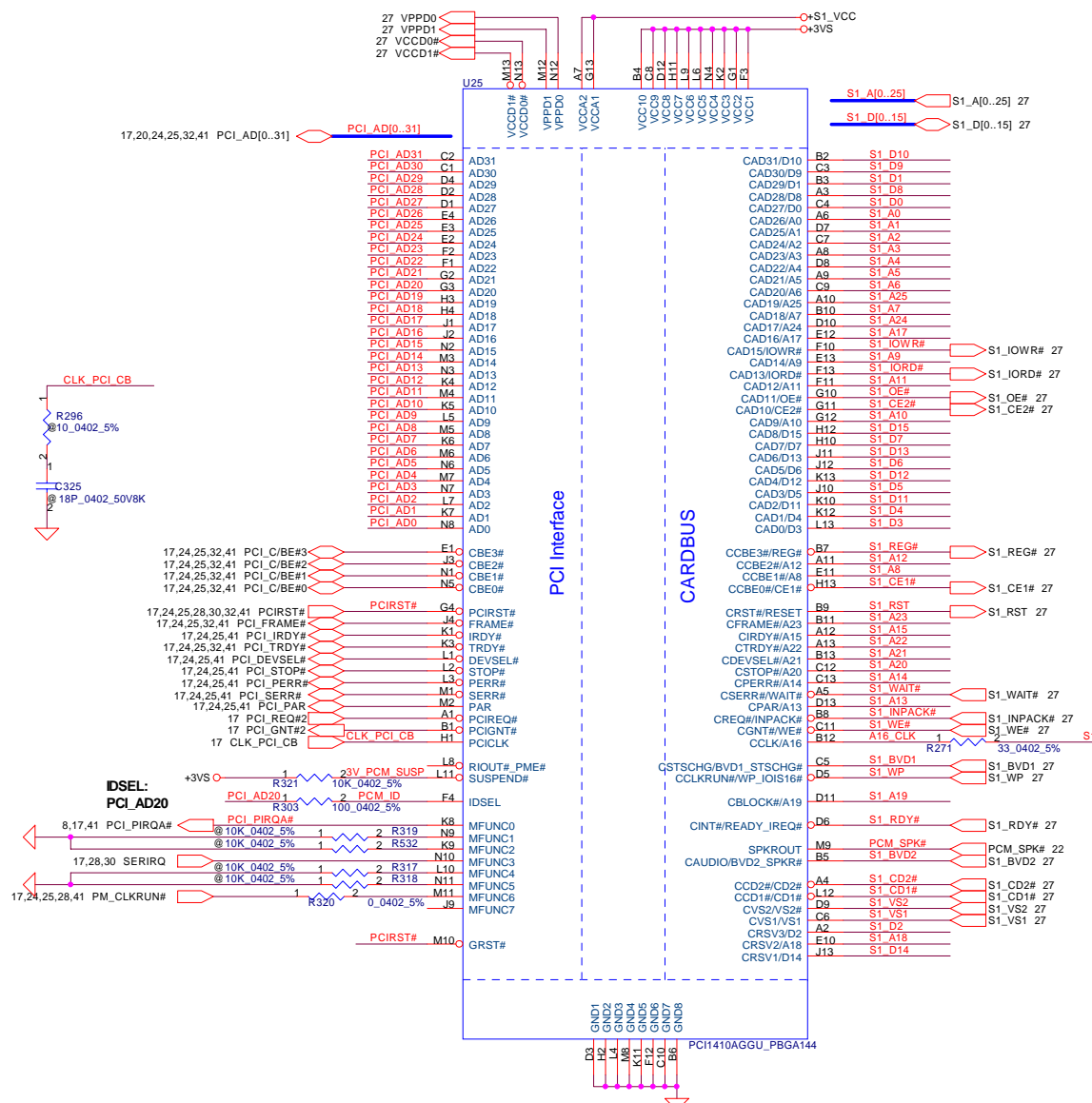


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				Sakhir 10E-HB110	
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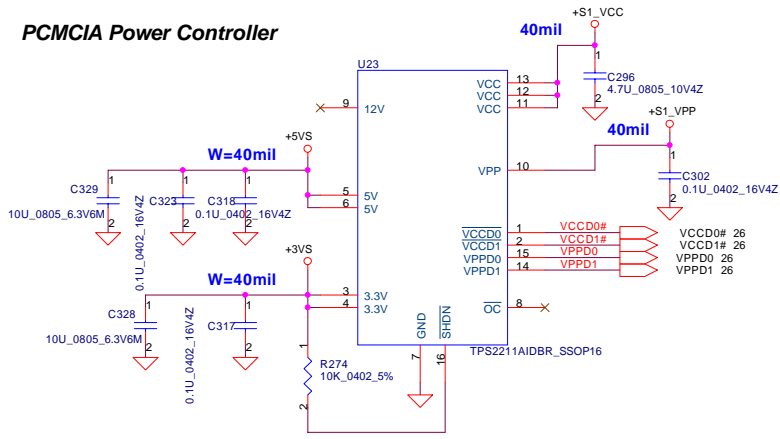


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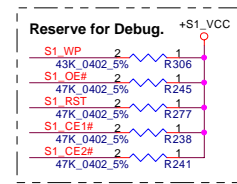
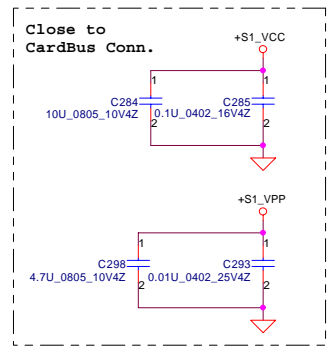
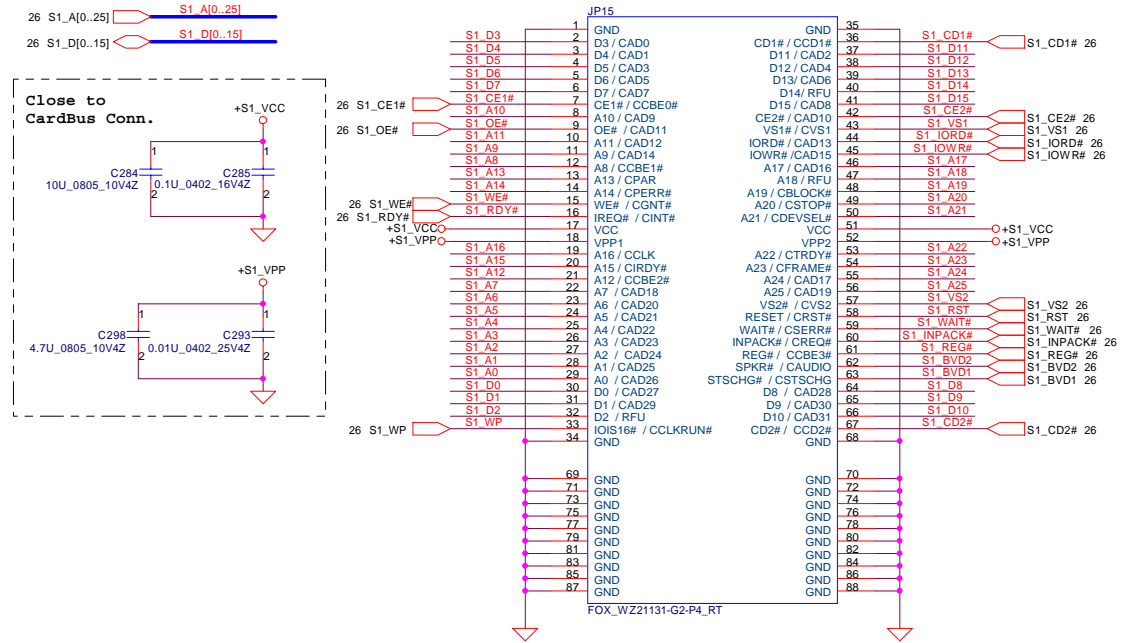


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PCMCIA Power Controller

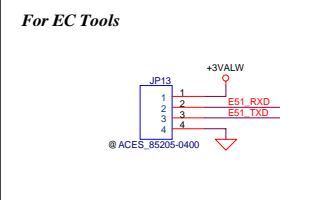
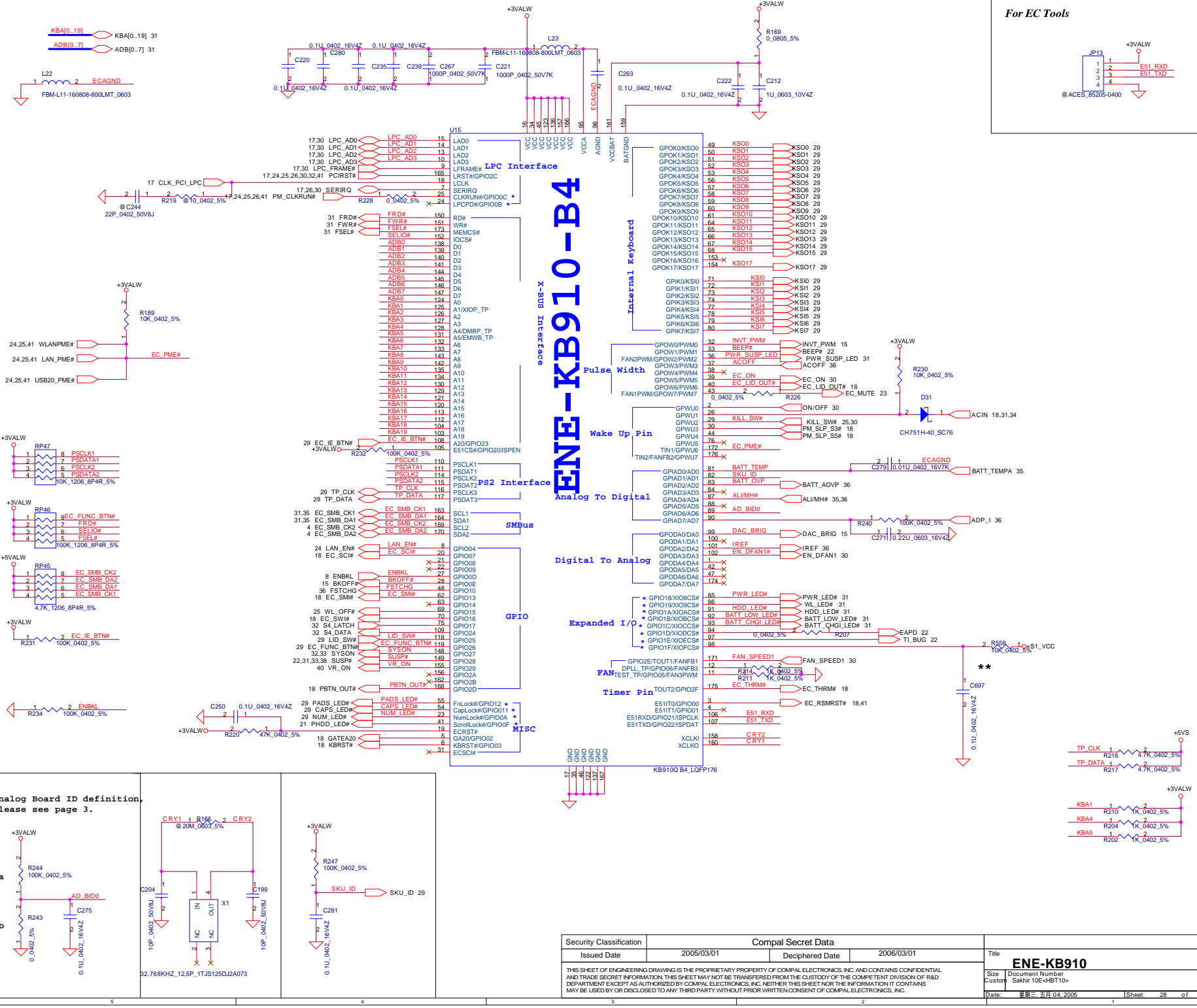


CardBus Socket

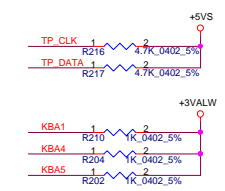
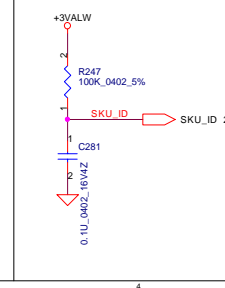
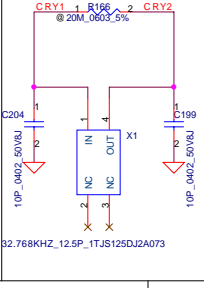
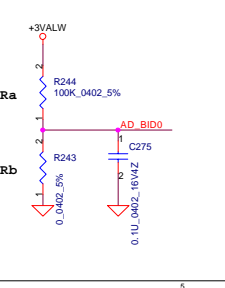


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ENE-KB910-B4

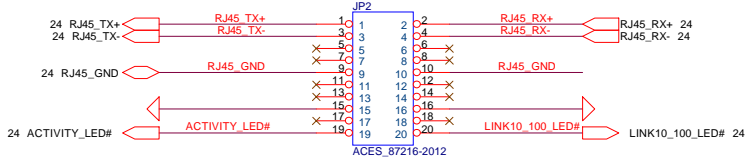


Analog Board ID definition, Please see page 3.

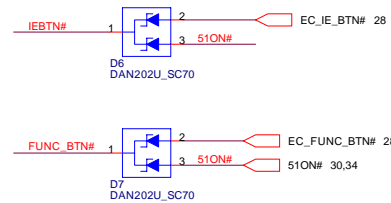
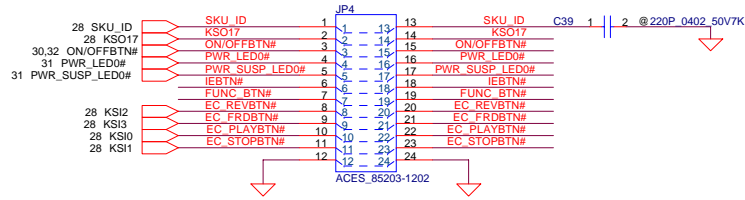


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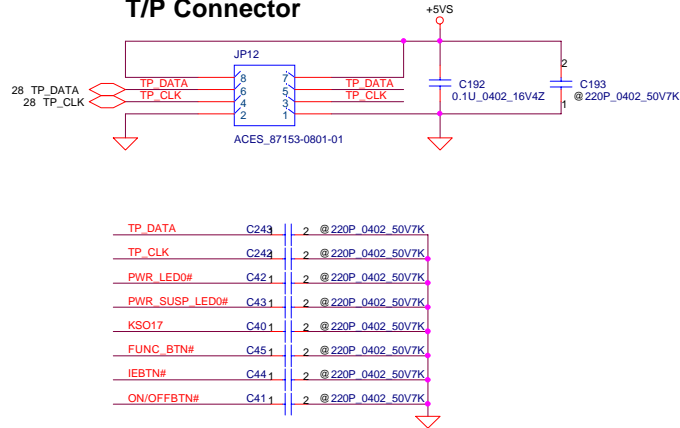
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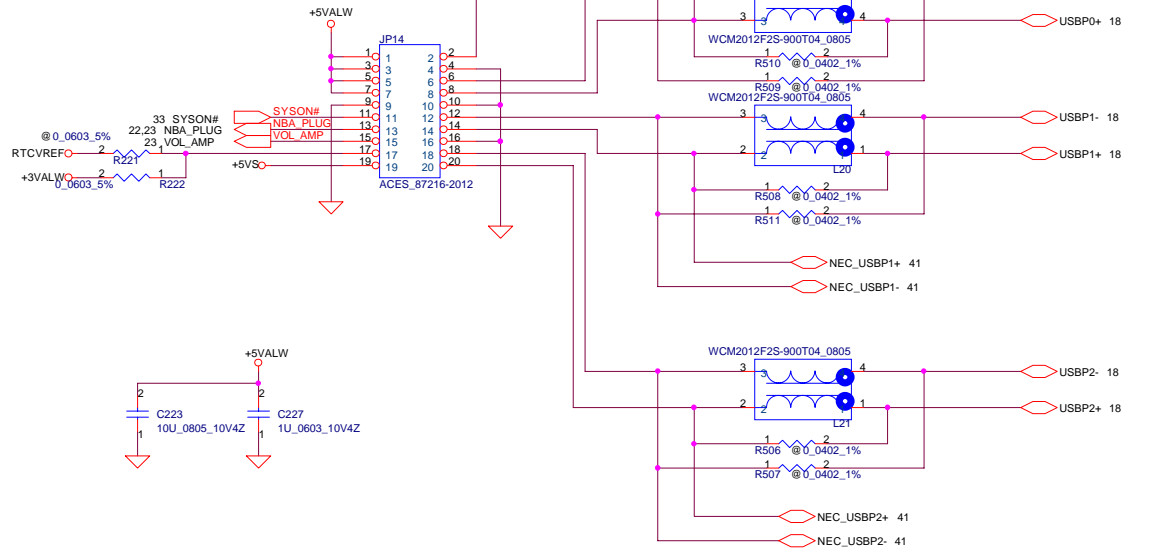
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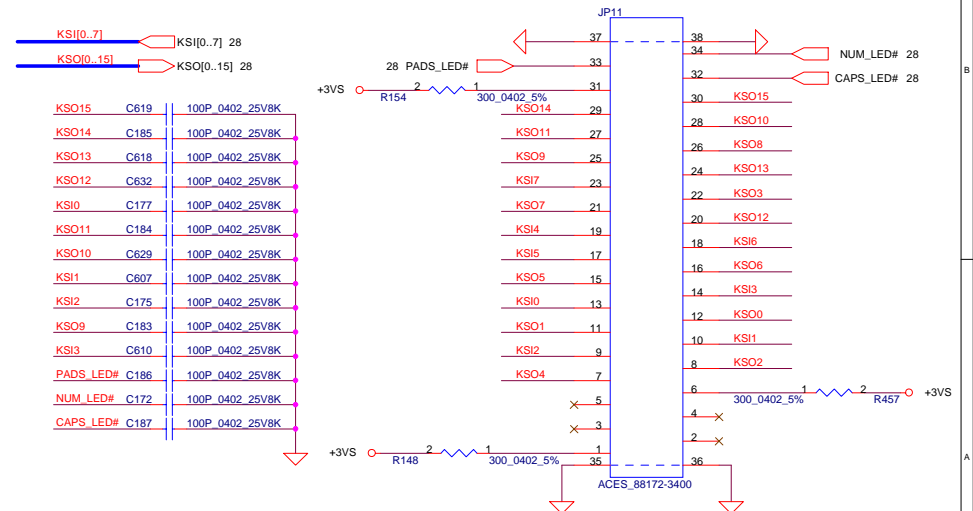
T/P Connector



USB Board Conn.

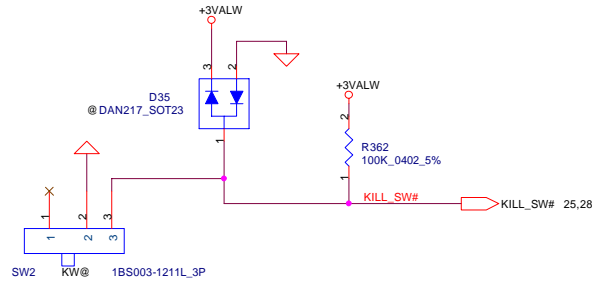


INT_KBD CONN.

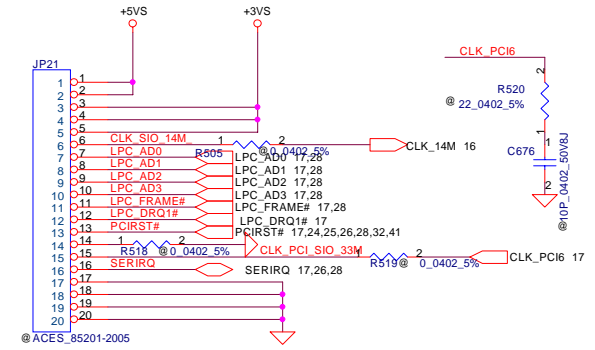


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				Rev 1.0
				Date: 星期三, 五月 04, 2005
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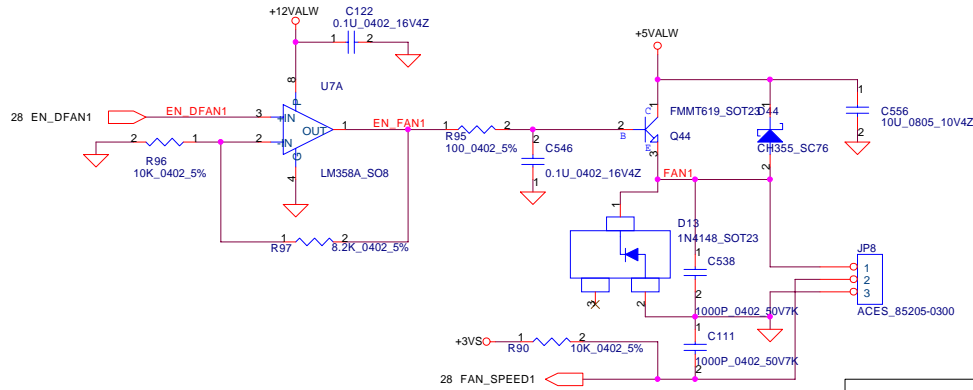
Kill SWITCH



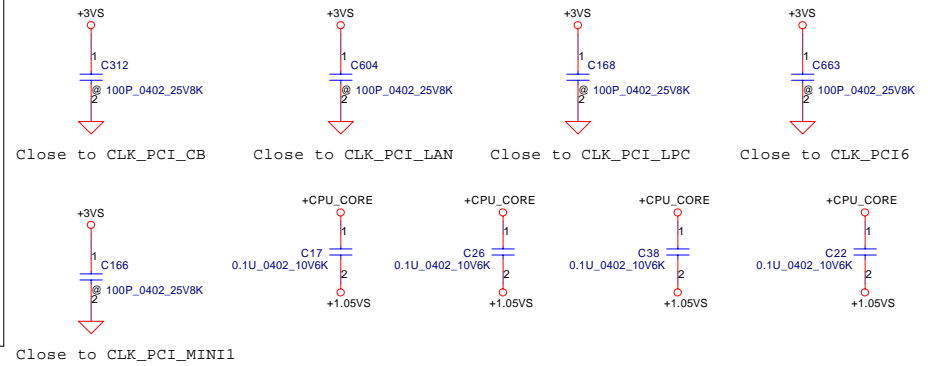
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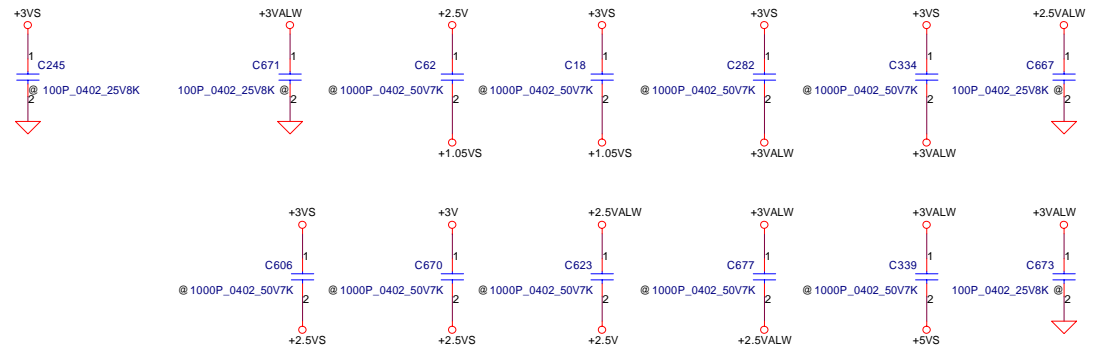
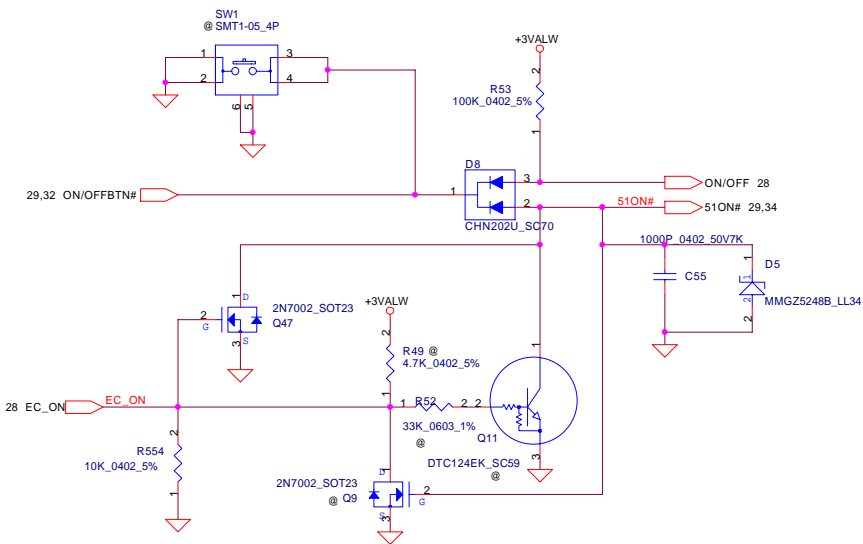
FAN CONN.



For EMI solution

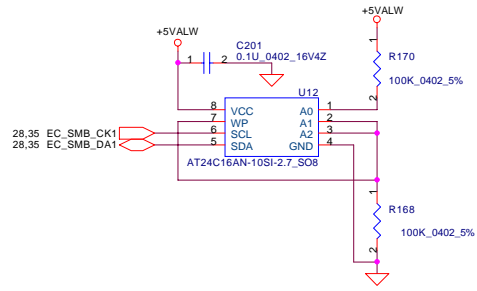


Power Button

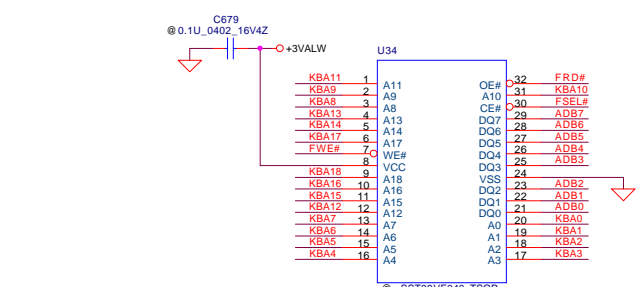
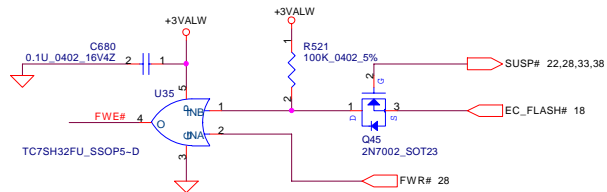


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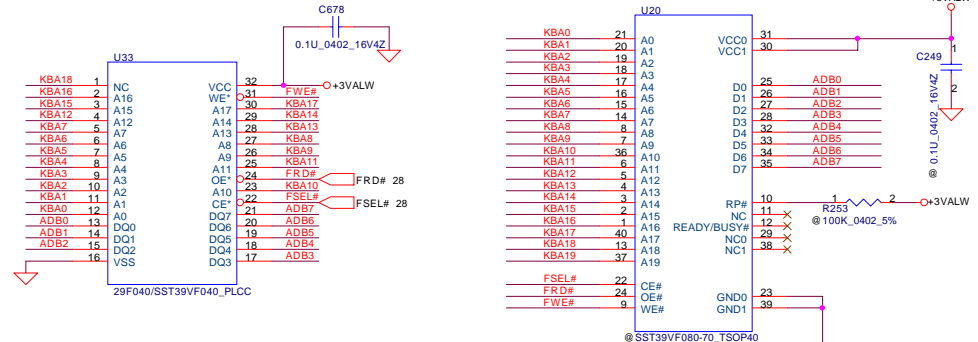
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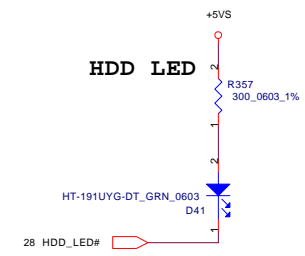
System BIOS



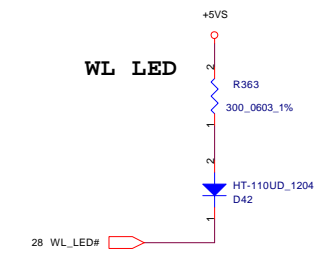
1MB Flash ROM



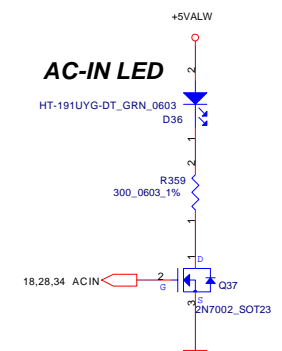
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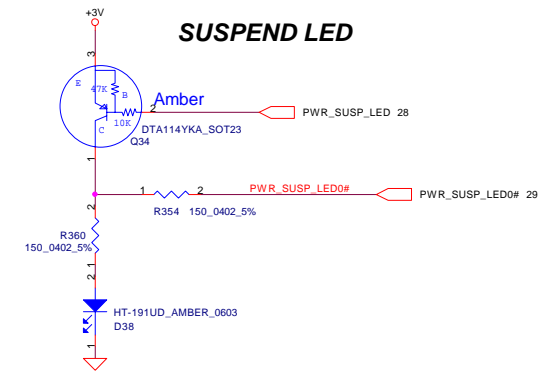
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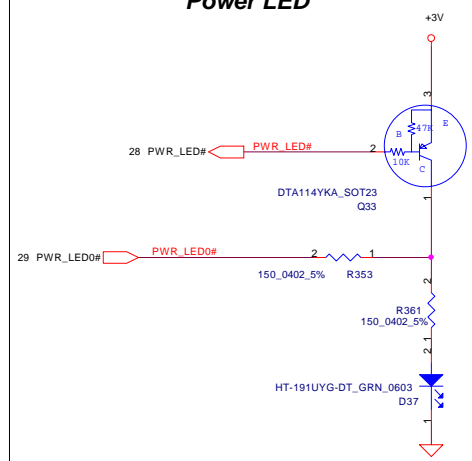
AC-IN LED



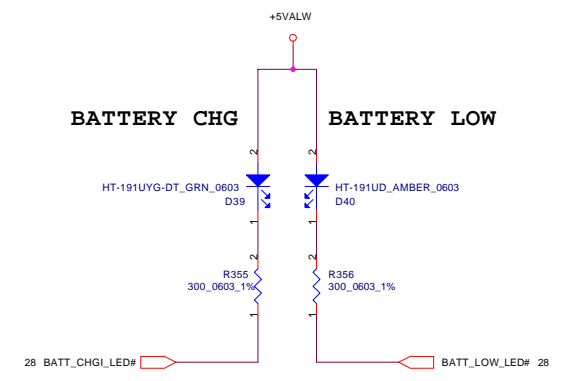
SUSPEND LED



Power LED

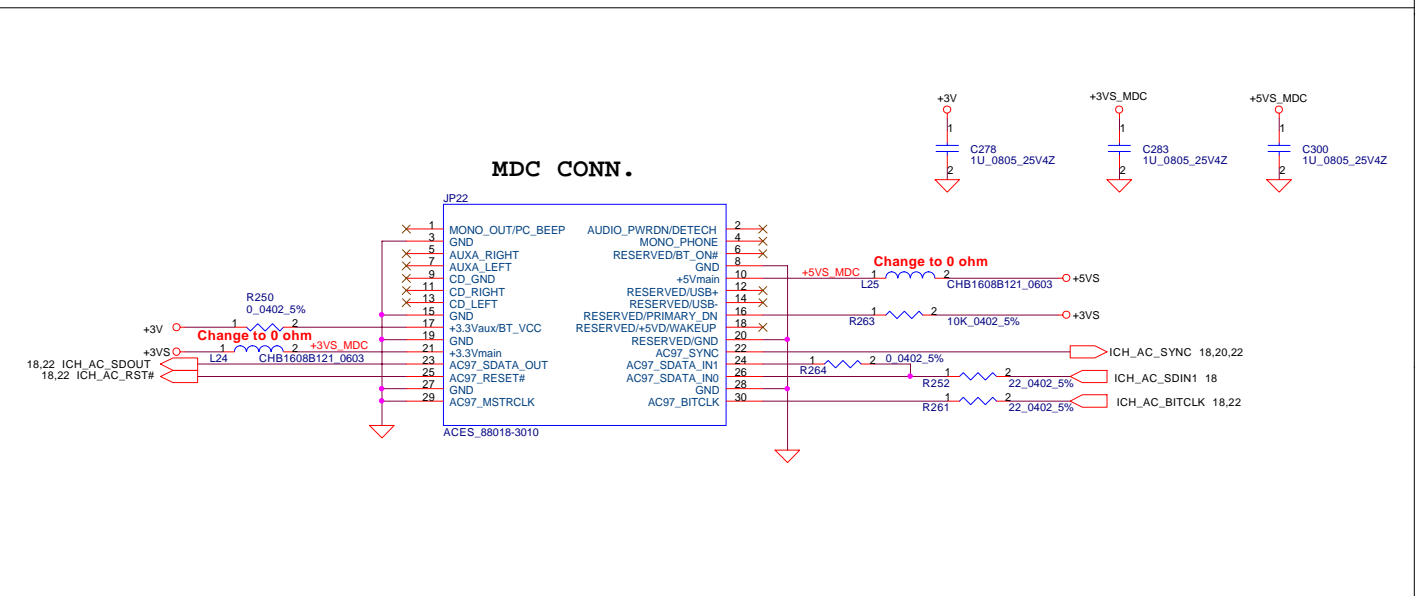
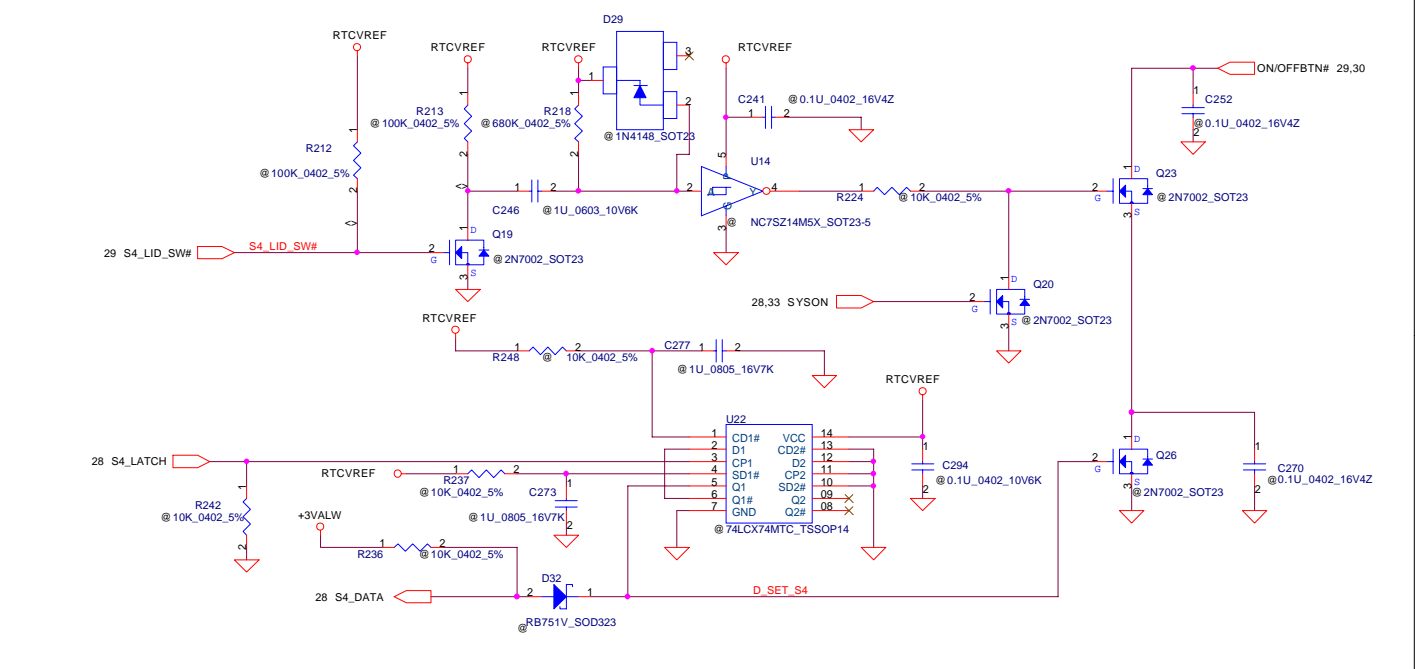
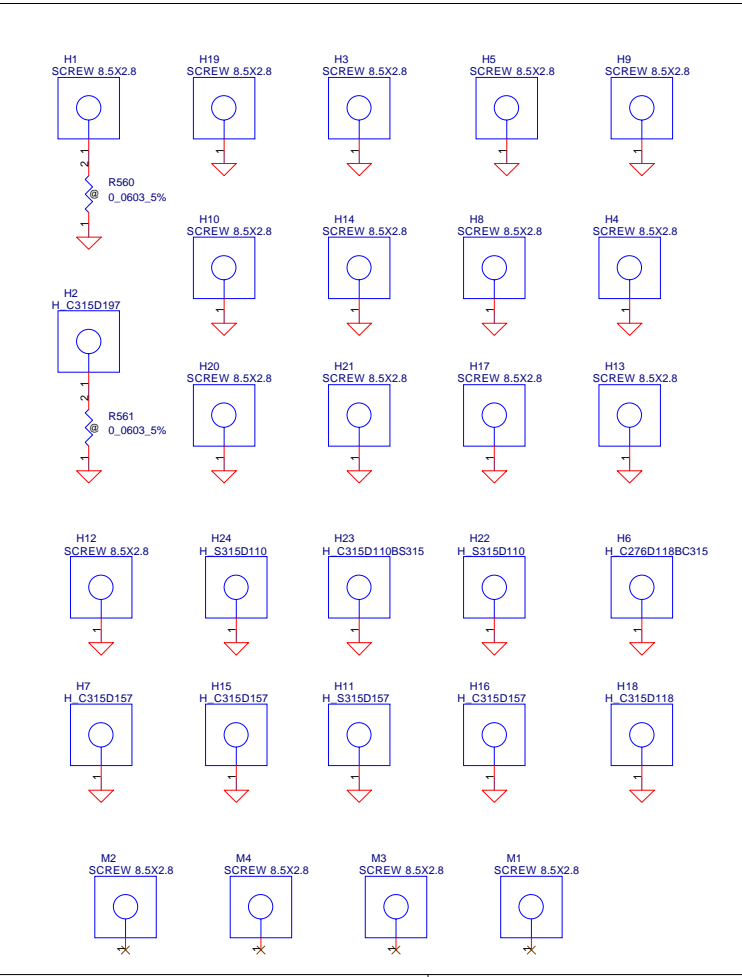
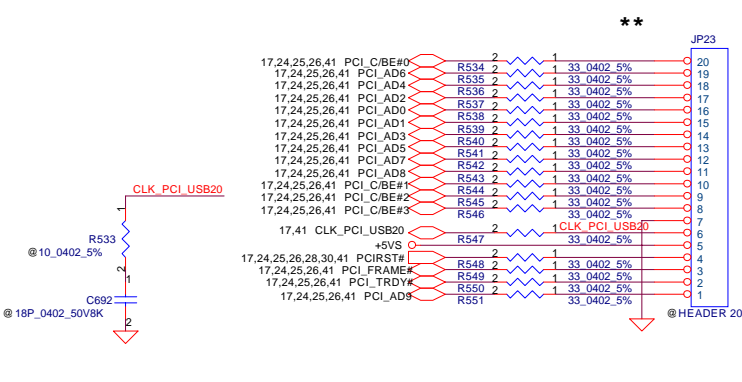


Battery LED

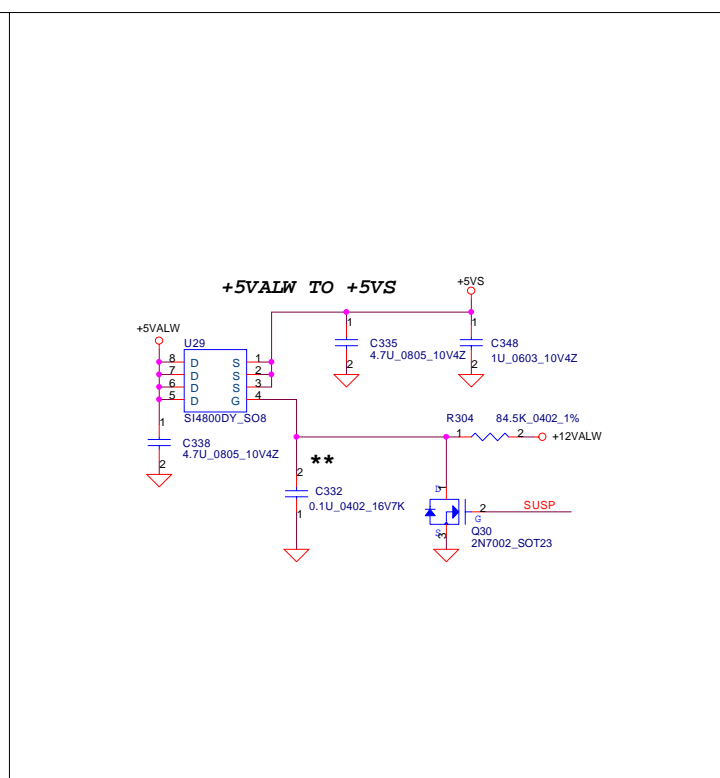
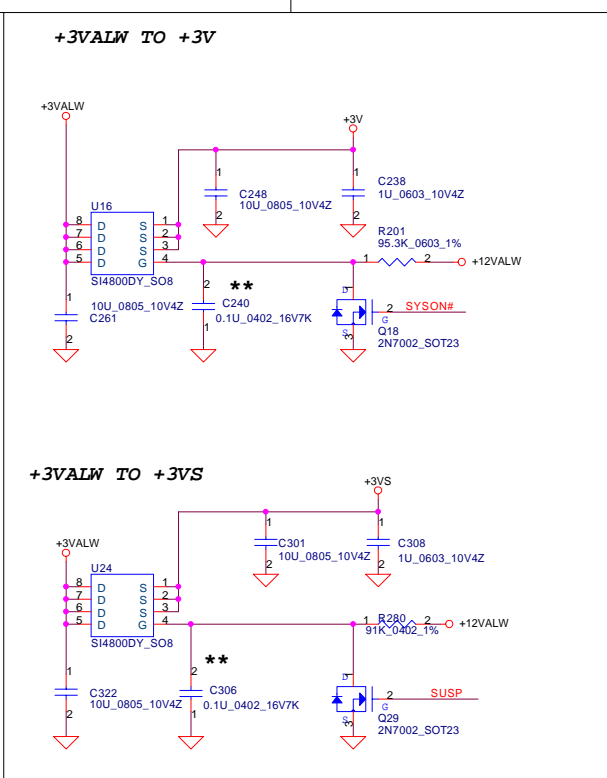
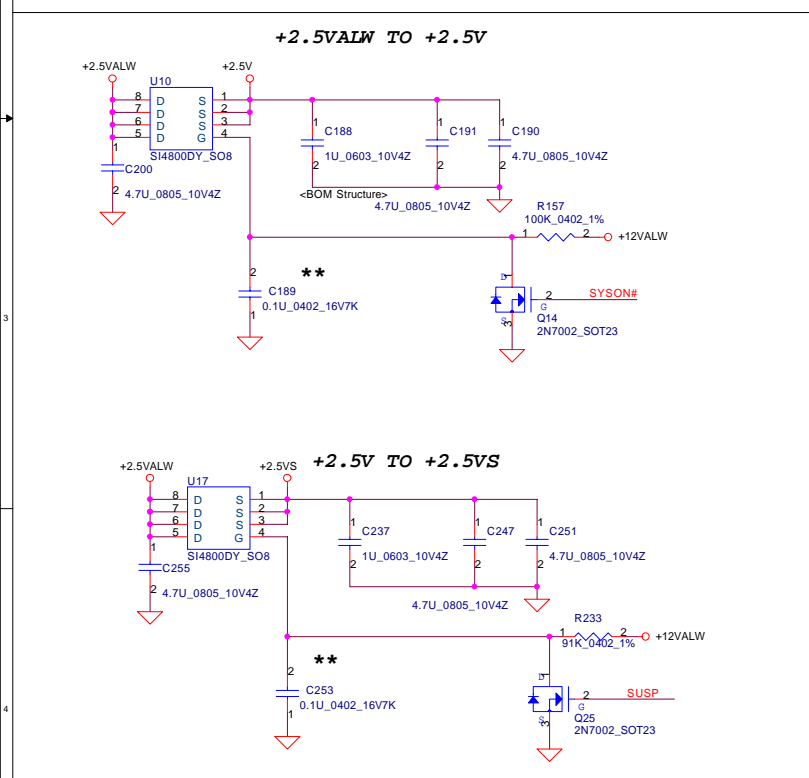
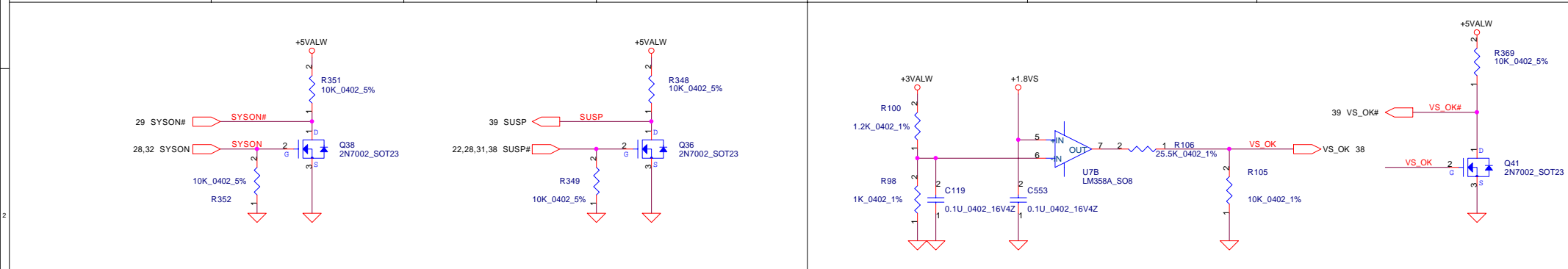
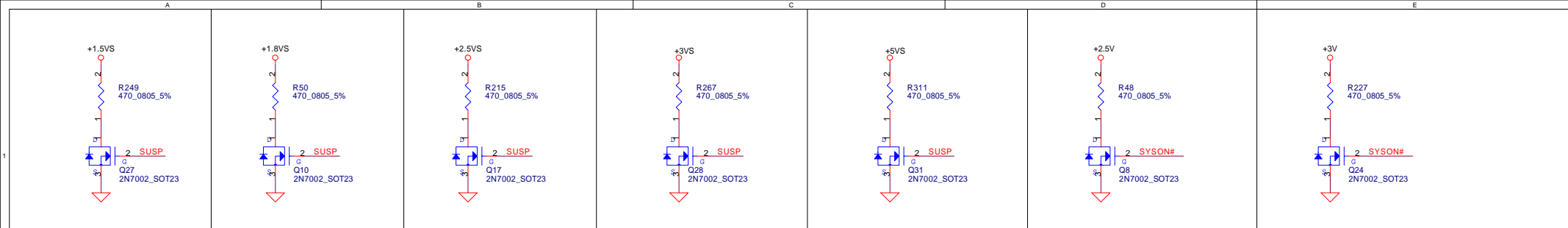


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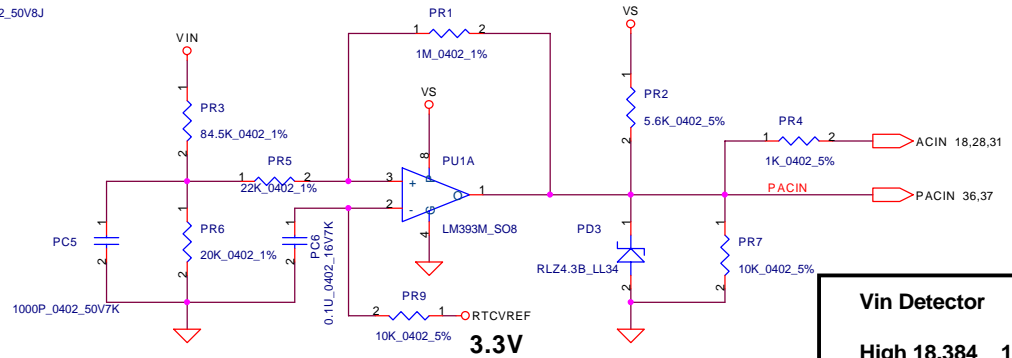
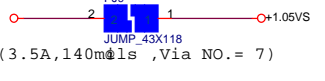
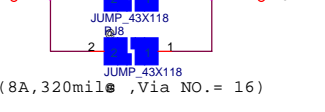
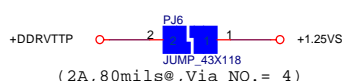
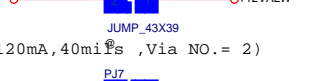
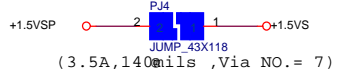
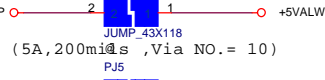
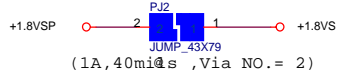
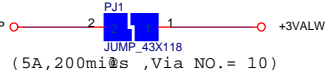
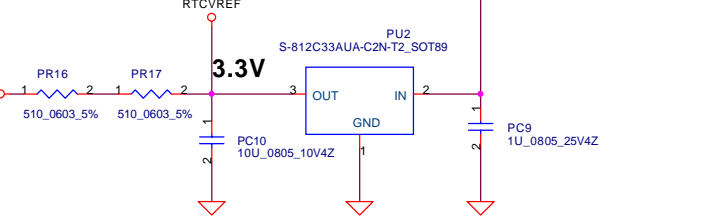
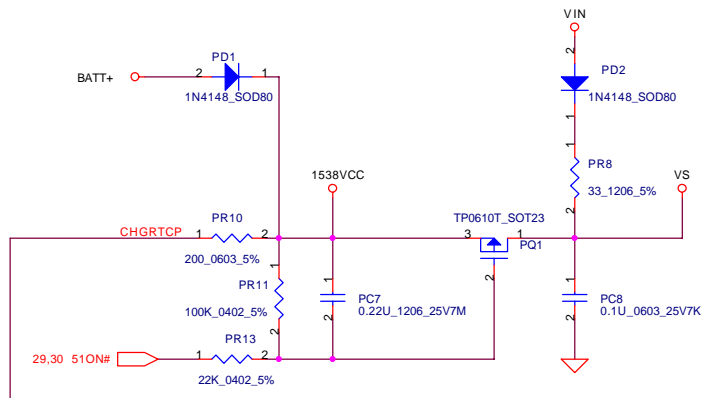
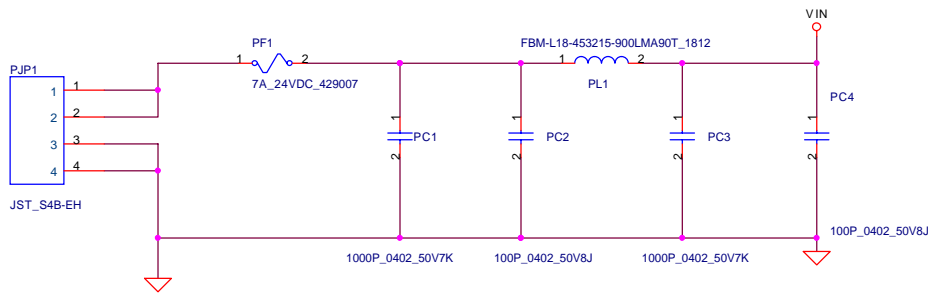
Port 80 Debug Card Connector



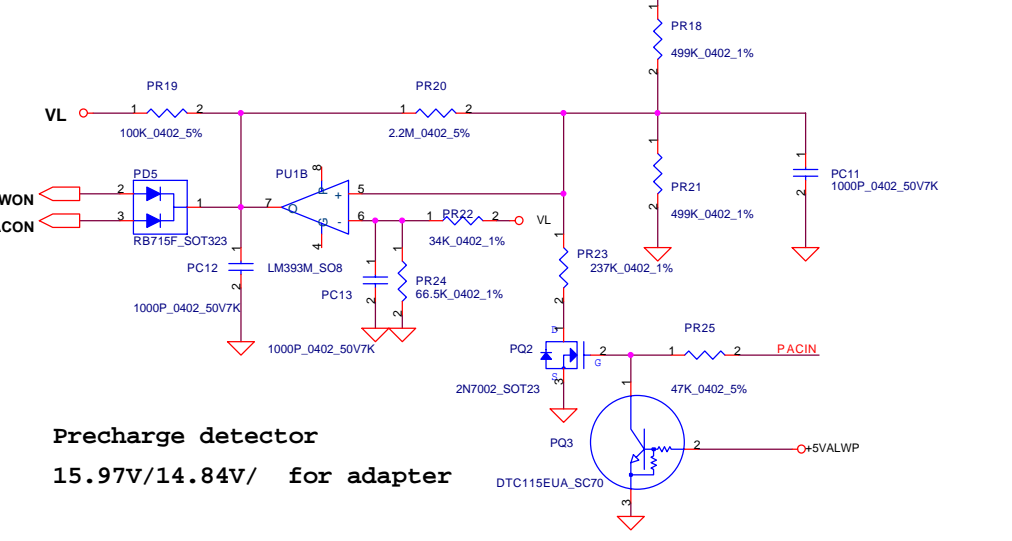
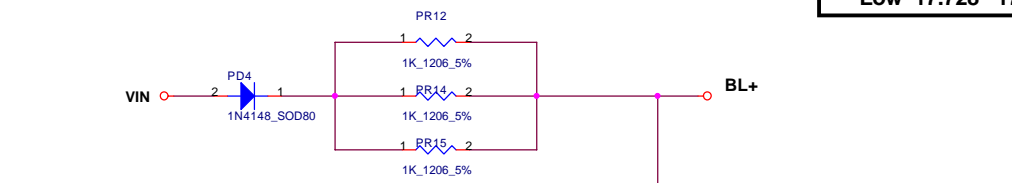
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				Rev	1.0
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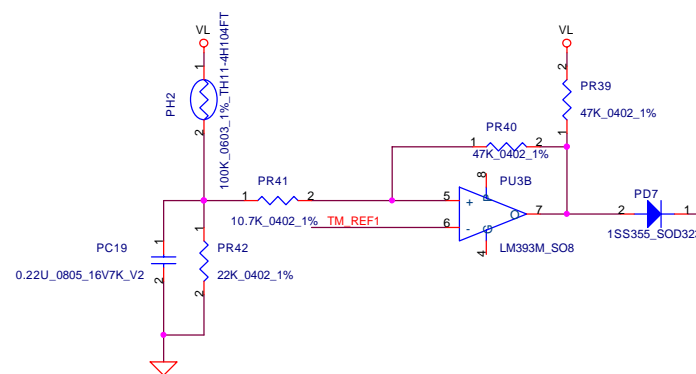
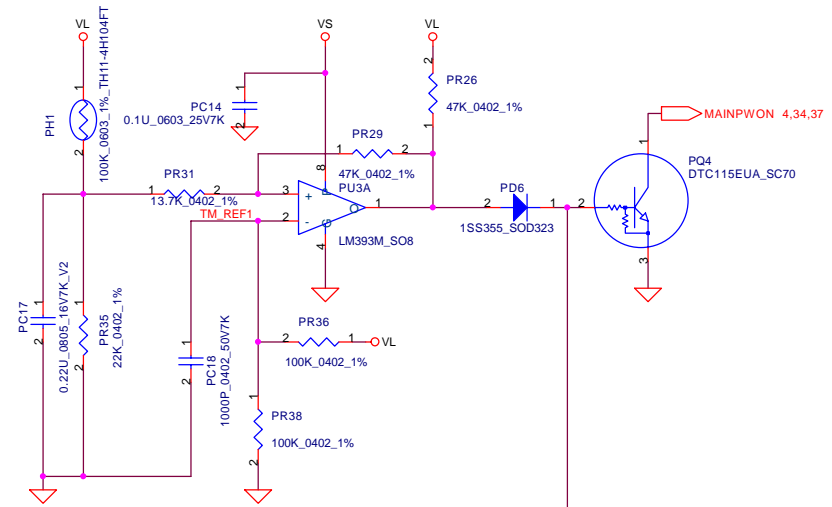
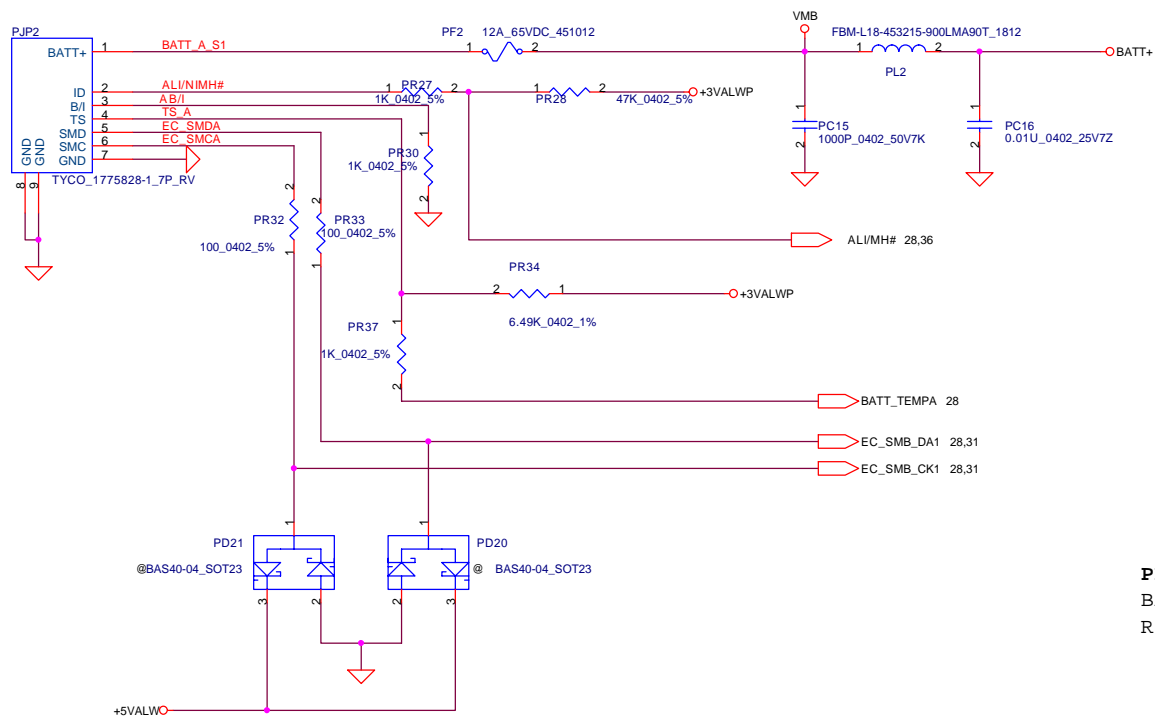


Vin Detector		
High	18.384	17.901 17.430
Low	17.728	17.257 16.976

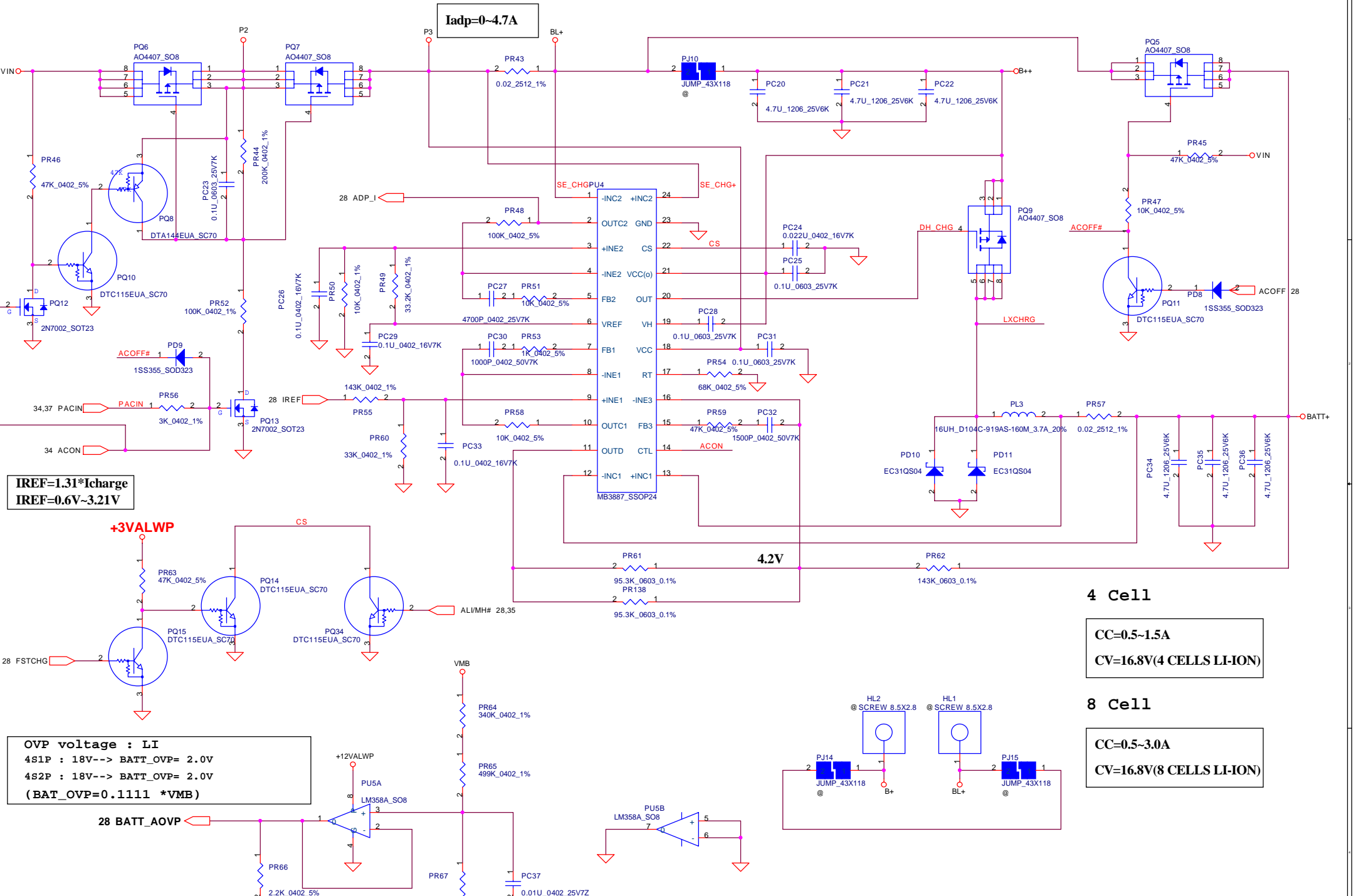


Precharge detector
15.97V/14.84V/ for adapter

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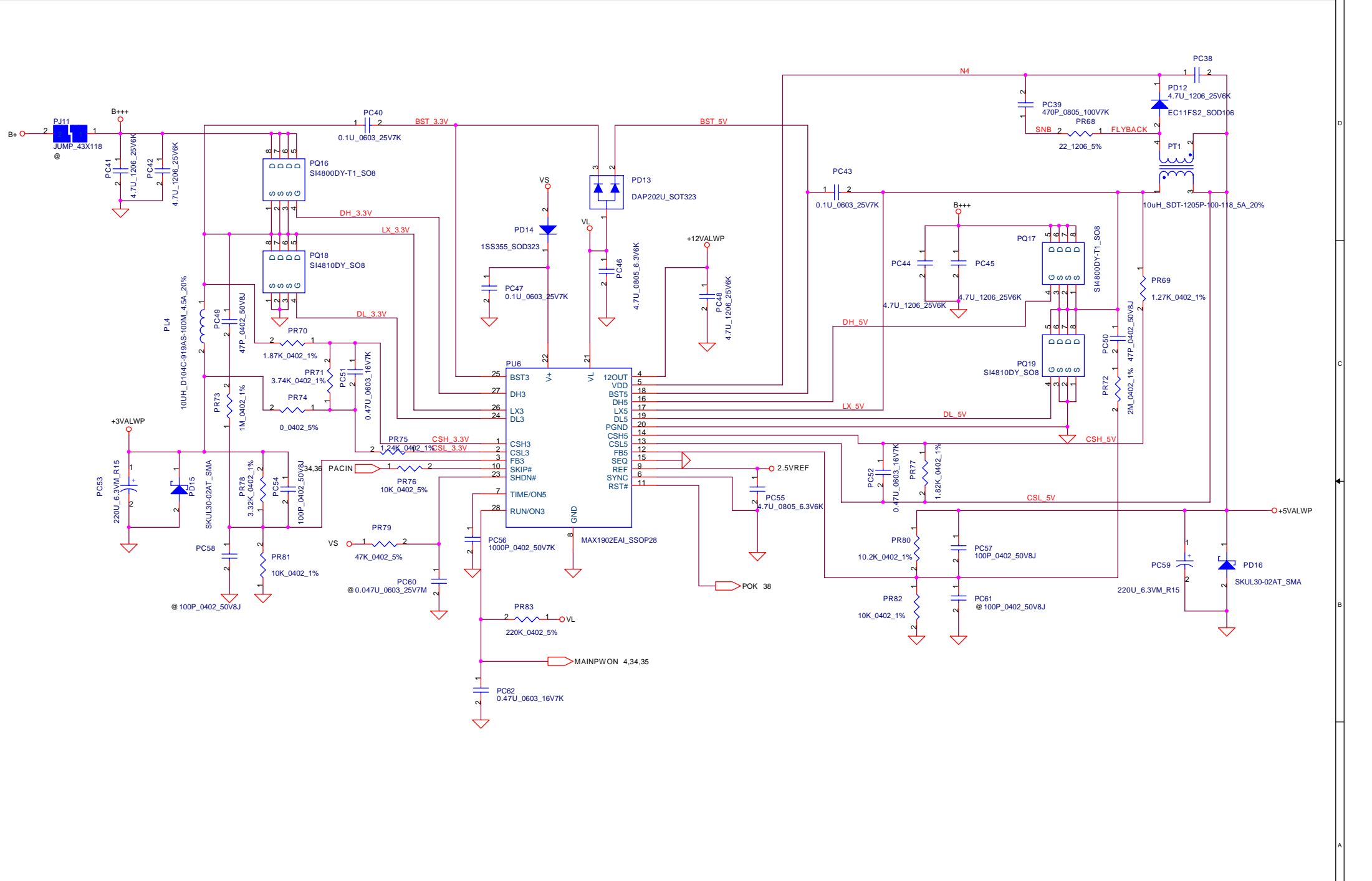
IREF=1.31*Icharge
IREF=0.6V~3.21V

OVP voltage : LI
4S1P : 18V--> BATT_OVP= 2.0V
4S2P : 18V--> BATT_OVP= 2.0V
(BATT_OVP=0.1111 *VMB)

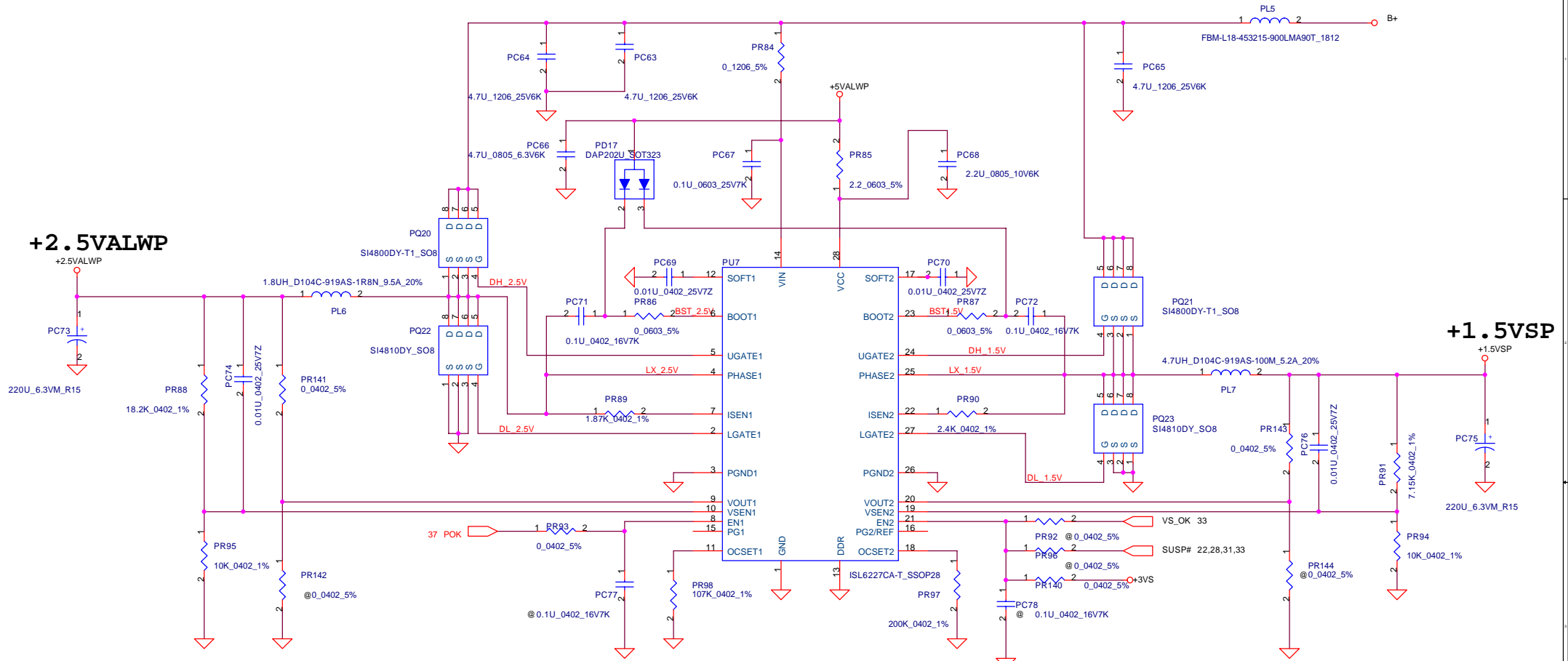
4 Cell
CC=0.5-1.5A
CV=16.8V(4 CELLS LI-ION)

8 Cell
CC=0.5-3.0A
CV=16.8V(8 CELLS LI-ION)

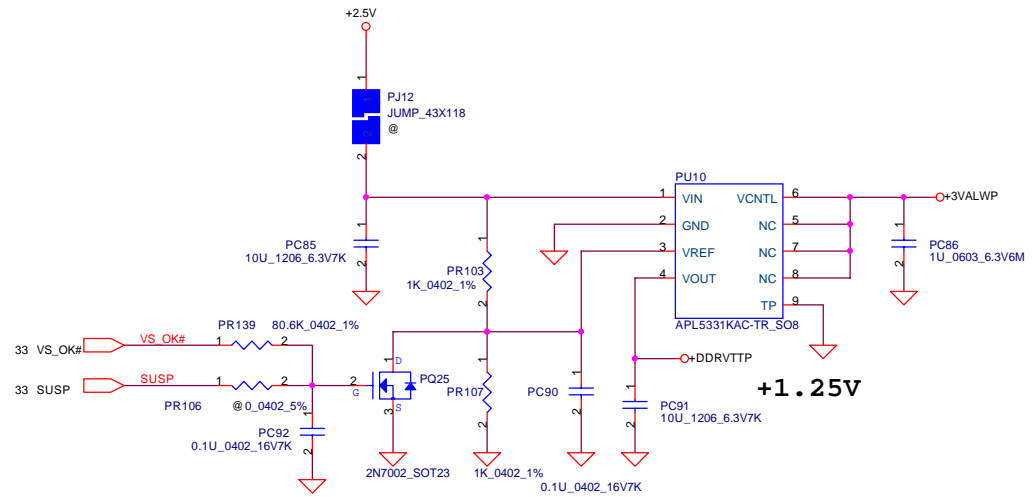
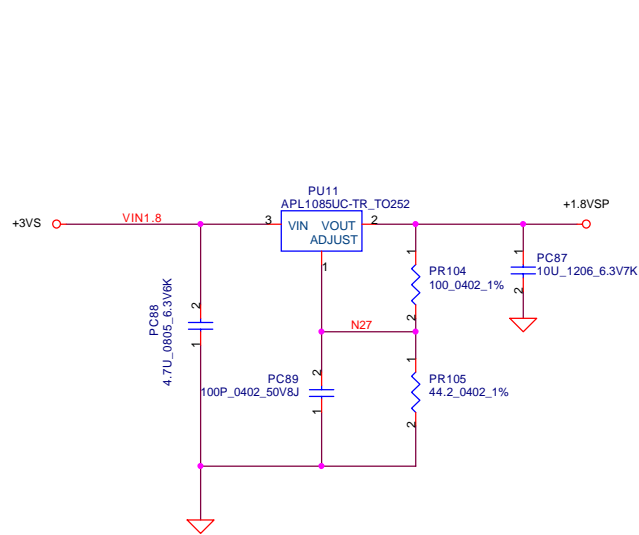
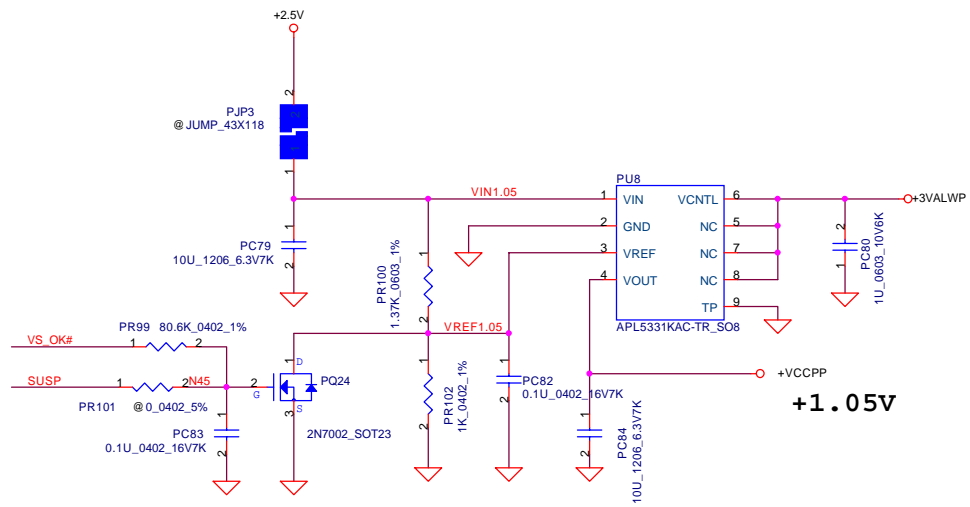
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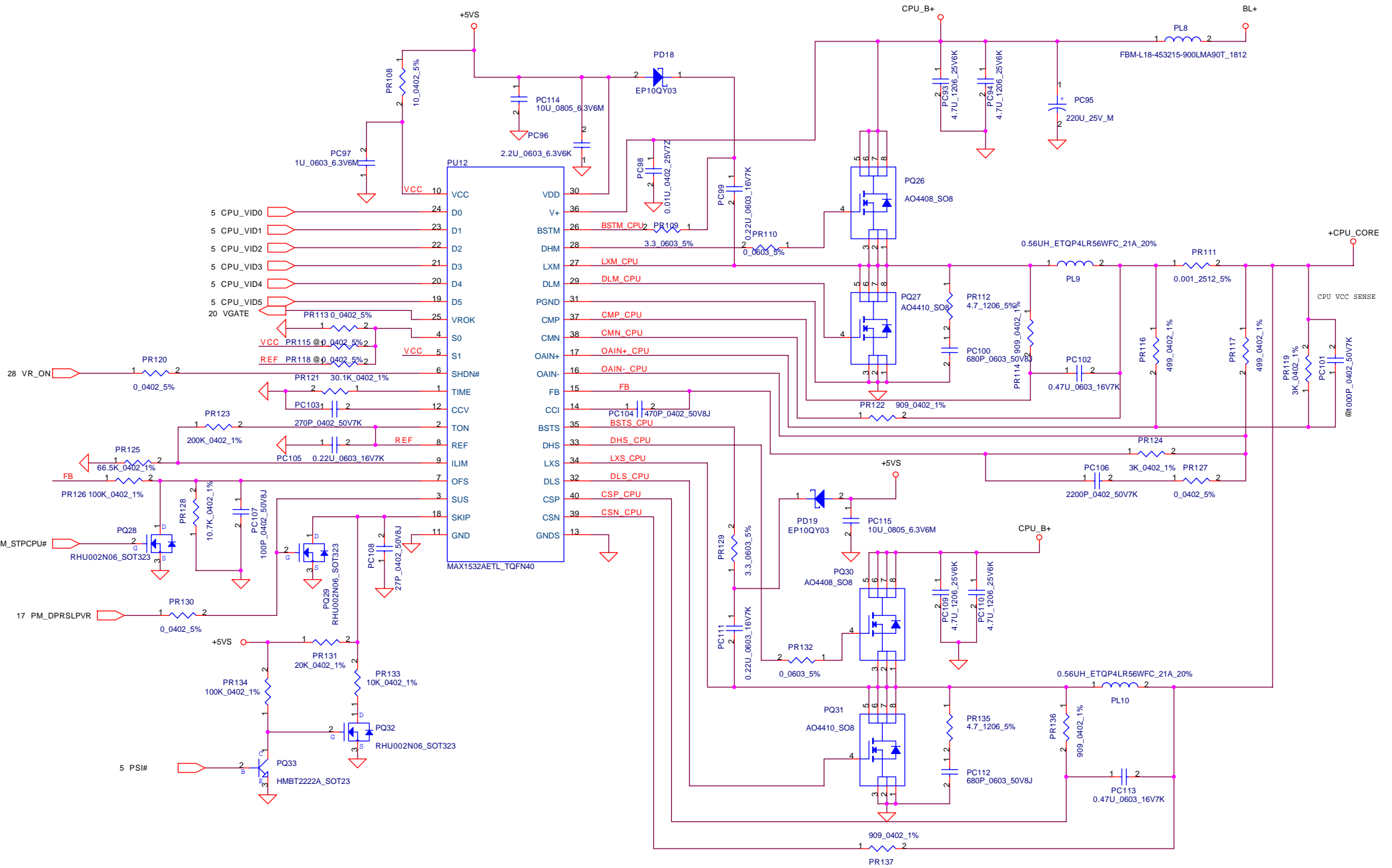
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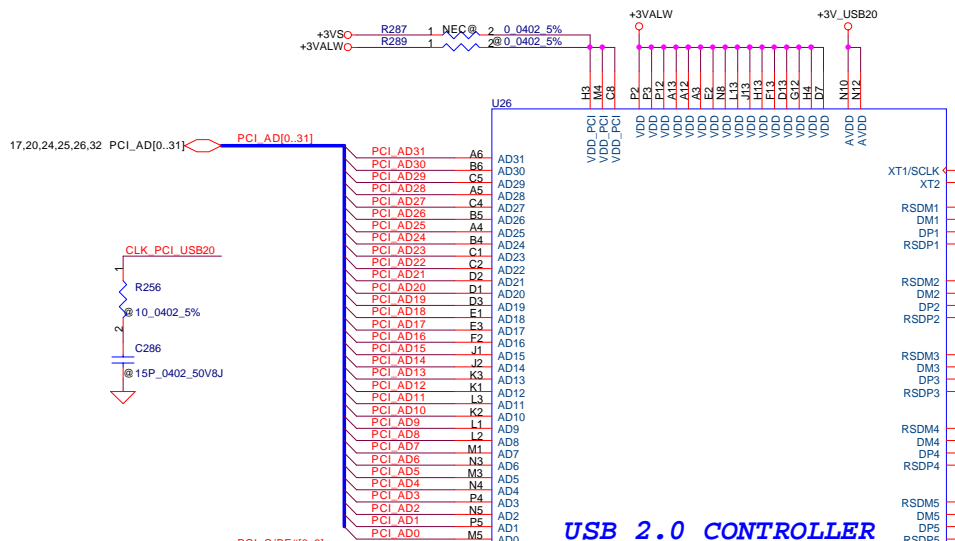
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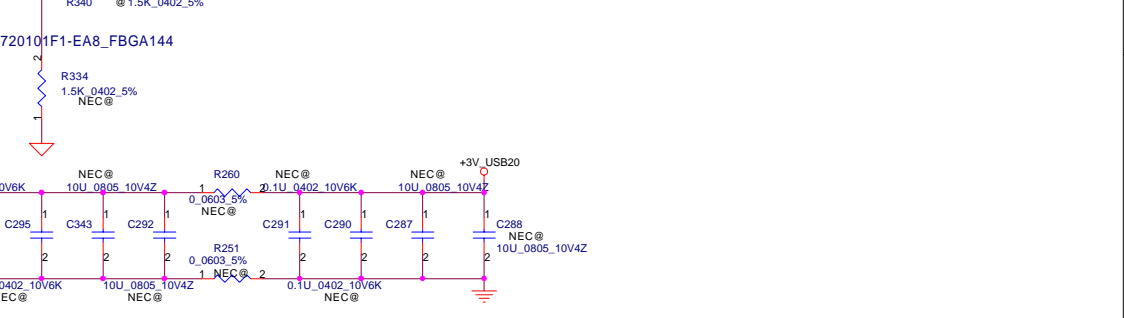
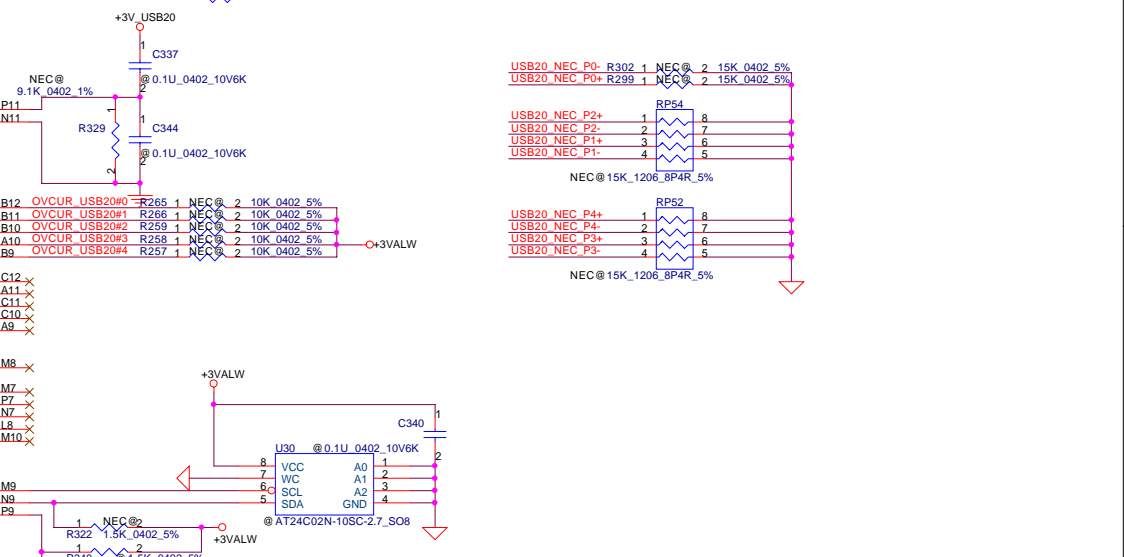
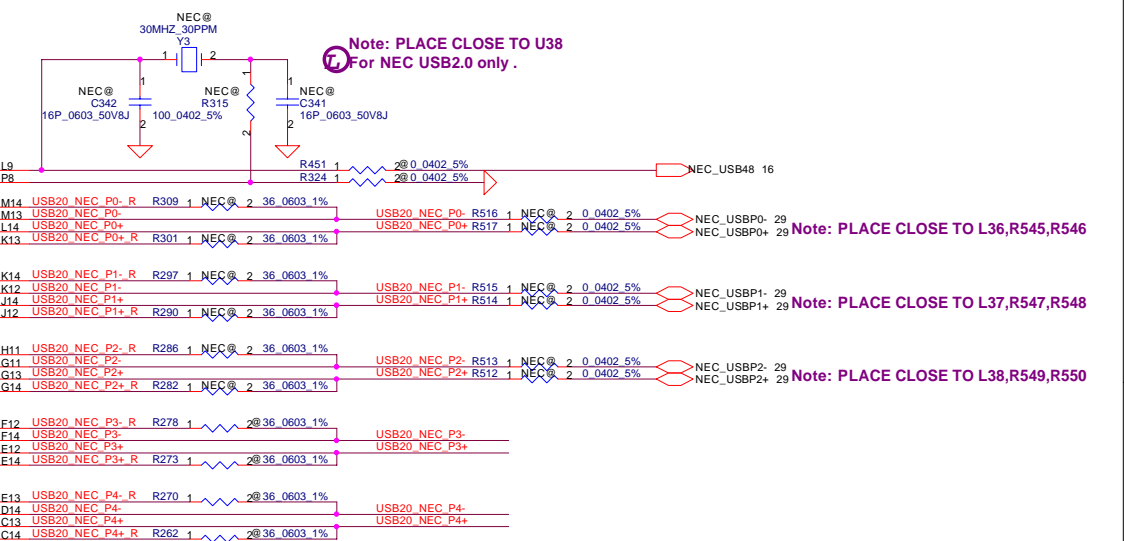
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USB 2.0 CONTROLLER
uPD72010F1-EA8
FBGA144



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LA-2811

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Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Description	Rev.
1	23	Design change	04/07/2005	Compal	Add Q46,R552,R553,D46 for Audio noise issue	0.2
2	5	Design change	04/07/2005	Compal	Del C46,C47	0.2
3	15	Design change	04/07/2005	Compal	Del R12 Add U3,C11 for backlight flash issue	0.2
4	17	Design change	04/12/2005	Compal	Change R136,R456,R142,R140,R134 from 33 to 390hm for EMI issue	0.2
5	22	Design change	04/12/2005	Compal	Add R555 for TI1410 bug.	0.2
6	23	Design change	04/07/2005	Compal	Del R510,R509,R508,R511,R506,R507 Add L19,L20,L21 for EMI solution	0.2
7	32	Design change	04/07/2005	Compal	Add R534-R551 for bebug port.	0.2
8	33	Design change	04/12/2005	Compal	Change R304 to 84.5K,R280,R233 to 91K,R157 to 100k for power sequence.	0.2
9	22	Design change	04/19/2005	Compal	Add R331,R310 for EMI. Change R293 from 33 to 390hm for EMI.	0.3
10	16	Design change	04/19/2005	Compal	Change R416,R422 from 33 to 390hm for EMI	0.3
11	28	Design change	04/29/2005	Compal	Add R558,C697 for TI bug	1.0

